(19)日本国特許庁（ＪＰ）　(12)特　許　公　報（Ｂ１）　(11)特許番号

第2978477号

(45)発行日　平成11年(1999)11月15日　(24)登録日　平成11年(1999)９月10日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　27/115		Ｈ０１Ｌ　27/10	４３４
21/8247		29/78	３７１
29/788			
29/792			

請求項の数19(全 33 頁)

(21)出願番号　特願平10－165733

(22)出願日　平成10年(1998)６月12日

審査請求日　平成10年(1998)６月12日

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(54)【発明の名称】　半導体集積回路装置およびその製造方法

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(57)【特許請求の範囲】

【請求項１】　第１導電型の半導体基板上に形成されたゲート絶縁膜上にワード線と電気的に接続されたゲート電極が形成され、前記半導体基板内にソース、ドレインを構成する第２導電型の第１、第２半導体領域が形成され、前記第１半導体領域と前記第２半導体領域との間にチャネル領域が形成されるＭＩＳＦＥＴによって不揮発性のメモリセルが構成された半導体集積回路装置であって、

前記ゲート絶縁膜は、少なくとも前記第１半導体領域側が第１酸化シリコン膜、窒化シリコン膜および第２酸化シリコン膜を積層した３層の絶縁膜からなり、前記メモリセルの書き込みは、前記第２半導体領域を前記第１半導体領域よりも高電位にして行うことを特徴とする半導体集積回路装置。

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【請求項２】　半導体基板上に形成されたゲート絶縁膜上にワード線と電気的に接続されたゲート電極が形成され、前記半導体基板内にソース、ドレインを構成する第２導電型の第１、第２半導体領域が形成され、前記第１半導体領域と前記第２半導体領域との間にチャネル領域が形成されるＭＩＳＦＥＴによって不揮発性のメモリセルが構成された半導体集積回路装置であって、

前記ゲート絶縁膜は、少なくとも前記第１半導体領域側が第１酸化シリコン膜、窒化シリコン膜および第２酸化シリコン膜を積層した３層の絶縁膜からなり、前記第１半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度は、前記第２半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度よりも低く、前記第１半導体領域側でホットエレクトロンを発生させることにより、前記窒化シリコン膜に前記ホットエレクトロンを注

入することを特徴とする半導体集積回路装置。

【請求項３】　半導体基板上に形成されたゲート絶縁膜上にワード線と電気的に接続されたゲート電極が形成され、前記半導体基板内にソース、ドレインを構成する第２導電型の第１、第２半導体領域が形成され、前記第１半導体領域と前記第２半導体領域との間にチャネル領域が形成されるＭＩＳＦＥＴによって不揮発性のメモリセルが構成された半導体集積回路装置であって、

前記ゲート絶縁膜は、前記第１半導体領域側が第１酸化シリコン膜、窒化シリコン膜および第２酸化シリコン膜を積層した３層の絶縁膜からなり、前記第２半導体領域側が酸化シリコン膜からなり、前記第１半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度は、前記第２半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度と異なることを特徴とする半導体集積回路装置。

【請求項４】　請求項１または３記載の半導体集積回路装置であって、前記第１半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度は、前記第２半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度よりも低いことを特徴とする半導体集積回路装置。

【請求項５】　請求項１、２または４記載の半導体集積回路装置であって、前記ゲート絶縁膜は、前記第１半導体領域側が前記第１酸化シリコン膜、窒化シリコン膜および第２酸化シリコン膜を積層した３層の絶縁膜からなり、前記第２半導体領域側が酸化シリコン膜からなることを特徴とする半導体集積回路装置。

【請求項６】　請求項１～５のいずれか一項に記載の半導体集積回路装置であって、前記ゲート絶縁膜は、前記第１半導体領域側と前記第２半導体領域側とがほぼ同じ電気的容量膜厚を有していることを特徴とする半導体集積回路装置。

【請求項７】　請求項１、２、４、５または６記載の半導体集積回路装置であって、前記ゲート絶縁膜は、前記第１半導体領域側および前記第２半導体領域側が、前記第１酸化シリコン膜、窒化シリコン膜および第２酸化シリコン膜を積層した３層の絶縁膜からなることを特徴とする半導体集積回路装置。

【請求項８】　請求項１、３、４、５、６または７記載の半導体集積回路装置であって、前記メモリセルの書き込みは、前記ゲート絶縁膜の一部を構成する前記窒化シリコン膜中にホットエレクトロンを注入して行うことを特徴とする半導体集積回路装置。

【請求項９】　請求項１～８のいずれか一項に記載の半導体集積回路装置であって、前記ゲート絶縁膜の少なくとも一部を構成する前記３層の絶縁膜のうち、前記窒化シリコン膜の下層に形成された前記第１酸化シリコン膜の膜厚は、直接トンネル電流が流れる膜厚よりも厚いことを特徴とする半導体集積回路装置。

【請求項１０】　請求項１～９のいずれか一項に記載の

半導体集積回路装置であって、前記第２半導体領域は、その一端が前記ゲート電極の下部に延在する第１導電型の半導体領域と、その一端が前記ゲート電極から離間した第２導電型の半導体領域とからなり、前記第１半導体領域は、第２導電型で構成されていることを特徴とする半導体集積回路装置。

【請求項１１】　請求項１～１０のいずれか一項に記載の半導体集積回路装置であって、前記メモリセルの読み出しは、前記第１半導体領域を前記第２半導体領域よりも高電位にして行うことを特徴とする半導体集積回路装置。

【請求項１２】　請求項１～１０のいずれか一項に記載の半導体集積回路装置であって、前記メモリセルの読み出しは、前記第２半導体領域を前記第１半導体領域よりも高電位にして行うことを特徴とする半導体集積回路装置。

【請求項１３】　請求項１～１２のいずれか一項に記載の半導体集積回路装置であって、前記第１、第２半導体領域の一方の上部の絶縁膜に形成された第１接続孔に埋め込まれたプラグによってソース線が形成され、前記第１、第２半導体領域の他方の上部の前記絶縁膜に形成された第２接続孔に埋め込まれたプラグを介して、前記第１、第２半導体領域の他方にビット線が接続されていることを特徴とする半導体集積回路装置。

【請求項１４】　請求項１３記載の半導体集積回路装置であって、前記第１接続孔および前記第２接続孔は、前記ＭＩＳＦＥＴのゲート電極のスペースに対して自己整合で形成されていることを特徴とする半導体集積回路装置。

【請求項１５】　請求項１～１４のいずれか一項に記載の半導体集積回路装置であって、前記メモリセルは、記憶素子部を構成する前記ＭＩＳＦＥＴと、選択用のＭＩＳＦＥＴとで構成されていることを特徴とする半導体集積回路装置。

【請求項１６】　請求項１～９、１１～１５のいずれか一項に記載の半導体集積回路装置であって、前記第１半導体領域と前記第２半導体領域とは同一の導電型であることを特徴とする半導体集積回路装置。

【請求項１７】　以下の工程を含むことを特徴とする半導体集積回路装置の製造方法；

（ａ）半導体基板上に第２酸化シリコン膜を形成した後、前記第２酸化シリコン膜の上部に形成した導体膜をパターニングすることにより、ＭＩＳＦＥＴのゲート電極を形成する工程、

（ｂ）前記ゲート電極の上部を含む前記半導体基板上に第２窒化シリコン膜を形成した後、前記第２窒化シリコン膜の上部に第４酸化シリコン膜を形成する工程、

（ｃ）前記第４酸化シリコン膜および前記第２窒化シリコン膜をエッチングすることにより、前記ＭＩＳＦＥＴの前記ゲート電極の上部および側壁を露出させる工程、

（ｄ）前記第２酸化シリコン膜を等方的にエッチングすることにより、前記ゲート電極の下部の第１領域において、前記ゲート電極の下面と前記半導体基板とを露出させ、前記ゲート電極の下部の第２領域において、前記第２酸化シリコン膜を残す工程、

（ｅ）前記半導体基板を熱処理することにより、前記第１領域において、前記半導体基板の表面および前記ゲート電極の下面に第１酸化シリコン膜を形成する工程、

（ｆ）前記第１領域において、前記半導体基板の表面に形成された前記第１酸化シリコン膜と、前記ゲート電極の下面に形成された前記第１酸化シリコン膜との隙間を含む前記半導体基板上に第２窒化シリコン膜を形成する工程。

【請求項１８】　請求項１７記載の半導体集積回路装置の製造方法であって、前記ゲート電極の前記第１領域側の端部に自己整合的に不純物を導入して、前記半導体基板内に第１半導体領域を形成する工程と、前記ゲート電極の前記第２領域側の端部に自己整合的に不純物を導入して、前記半導体基板内に第２半導体領域を形成する工程とを含み、前記第１半導体領域の不純物濃度を前記第２半導体領域の不純物濃度よりも低くすることを特徴とする半導体集積回路装置の製造方法。

【請求項１９】　請求項１７または１８記載の半導体集積回路装置の製造方法であって、前記ＭＩＳＦＥＴは不揮発性メモリを構成し、周辺回路を構成するＭＩＳＦＥＴのゲート電極と、前記不揮発性メモリを構成するＭＩＳＦＥＴのゲート電極とは、同一の導電膜をパターニングする工程で形成され、前記周辺回路を構成するＭＩＳＦＥＴのゲート絶縁膜は、前記第２酸化シリコン膜を形成する工程で形成されることを特徴とする半導体集積回路装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体集積回路装置およびその製造技術に関し、特に、絶縁膜トラップを電荷の蓄積領域とした単一ＭＩＳＦＥＴ構造の不揮発性メモリを有する半導体集積回路装置に適用して有効な技術に関する。

【０００２】

【従来の技術】シリコン基板上に形成される不揮発性メモリの基本セル構造は、ゲート酸化膜とその上部のコントロールゲート（ワード線）との間に設けられ、周囲と電気的に絶縁されたフローティング（浮遊）ゲートを電荷の蓄積領域とする、いわゆるフローティングゲート型と、このようなフローティングゲートを持たず、ゲート絶縁膜が酸化シリコン膜と窒化シリコン膜との積層膜で構成され、上記窒化シリコン膜中にトラップされた電子を電荷の蓄積領域とするＭＮＯＳ(Metal-gate Nitride Oxide Silicon)型とに大別される。

【０００３】図５２は、フローティングゲート型メモリセルの代表的なセル構造を示す断面図である。このメモリセルは、シリコン基板１０１の主面上に形成された膜厚１０nm程度のゲート酸化膜１０２の上部にフローティングゲート１０３、層間絶縁膜１０４およびコントロールゲート（ＣＧ）１０５を順次形成し、フローティングゲート１０３の両側のシリコン基板１０１にソース（Ｓ）１０６およびドレイン（Ｄ）１０７を形成した構造になっている。

【０００４】メモリセルの書き込みは、フローティングゲート１０３中に電子１０８を注入し、コントロールゲート１０５から見たトランジスタのしきい値電圧（Ｖｔｈ）を電子１０８の蓄積のない状態に比較して３Ｖ～５Ｖ程度上昇させることによって行う。また、フローティングゲート１０３への電子１０８の注入は、アバランシェ・ブレークダウンによって発生するドレイン１０７近傍のホットエレクトロンをコントロールゲート１０５に印加した正電圧によってフローティングゲート１０３へ引き込む方式が主流である。

【０００５】一方、図５３は、ＭＮＯＳ型メモリセルの代表的なセル構造を示す断面図である。このメモリセルは、シリコン基板１１１の主面上に形成された膜厚２nm程度の直接トンネル酸化膜１１２の上部に窒化シリコン膜１１３および書き込み／消去用のゲート電極（ＰＥＧ）１１５ａが順次形成され、ゲート電極１１５ａの両側のシリコン基板１１１にソース（Ｓ）１１６および接続拡散層（ドレイン）１１７が形成されたＭＩＳＦＥＴ（記憶素子部）と、ゲート酸化膜１１８の上部に選択用のゲート電極（ＳＧ）１１５ｂが形成され、ゲート電極１１５ｂの両側のシリコン基板１１１に接続拡散層（ソース）１１７およびドレイン（Ｄ）１１９が形成された選択用ＭＩＳＦＥＴとで構成されている。

【０００６】メモリセルの書き込みは、シリコン基板１１１および書き込み／消去用のゲート電極１１５ａの電位を制御し、直接トンネル酸化膜１１２を介してシリコン基板１１１側から窒化シリコン膜１１３中へ電子１０８を全面注入してトラップさせることにより、記憶素子部のＭＩＳＦＥＴのしきい値電圧を上昇させて行う。また、消去も同様に、シリコン基板１１１およびゲート電極１１５ａの電位を制御し、窒化シリコン膜１１３中にトラップさせた電子をシリコン基板１１１側へ放出することにより、記憶素子部のＭＩＳＦＥＴのしきい値電圧を下降させて行う。この消去動作の際には、記憶素子部のしきい値電圧を０Ｖ以下、すなわちデプレッション領域まで低下させるので、読み出しを行うためには記憶素子部のＭＩＳＦＥＴ以外に前記した選択用ＭＩＳＦＥＴが必要となる。

【０００７】上記ＭＮＯＳ型メモリセルは、絶縁膜（窒化シリコン膜１１３）中に電子をトラップさせる動作方式であることから、トラップされた電子はそれぞれ独立にしきい値電圧の変調に寄与している。そのため、直接

トンネル膜１１２中の欠陥に起因した窒化シリコン膜１１３中の電子の部分的な漏洩による、記憶素子部のチャネル全域にわたるしきい値電圧の変動が非常に小さい。言い替えると、リテンション特性が優れており、信頼度の高いメモリセル方式であると言える。

【０００８】図５４は、米国特許（ＵＳＰ）第５４０８１１５号に記載され、“Self-Aligned Split-Gate EEPROM Device”と名付けられたセル構造を示す断面図である。このメモリセルは、シリコン基板１２１の主面上にゲート酸化膜１２２および選択用ゲート電極（ＳＧ）１２３を積層し、それらの側壁部に酸化シリコン膜１２４、窒化シリコン膜１２５および酸化シリコン膜１２６からなる３層の絶縁膜を介してサイドウォールゲート電極（ＳＷＧ）１２７を形成した構造になっている。また、ソース（Ｓ）１２８は、このサイドウォールゲート電極（ＳＷＧ）１２７をマスクとするイオン注入により形成され、ドレイン（Ｄ）１２９は、前記選択用ゲート電極１２３をマスクとするイオン注入により形成されている。

【０００９】メモリセルの書き込みは、“1997 Symposium on VLSI Technology Digest ofTechnical Papers p63-p64”に記載されているように、ドレイン１２９を接地電位とし、ソース１２８、サイドウォールゲート電極１２７および選択ゲート電極１２３にそれぞれ５Ｖ、９Ｖ、１Ｖの電圧を印加することによって行う。

【００１０】図５５は、上記メモリセルの書き込み動作時におけるチャネル領域の電位分布と電界強度分布とを示している。ソース（Ｓ）－ドレイン（Ｄ）間に印加された電圧（５Ｖ）は、その大半がソース（Ｓ）の空乏層に印加されるので、図示のように、チャネル方向に沿った電界強度はサイドウォールゲート電極（ＳＷＧ）の直下において最大値となる。そのため、ドレイン（Ｄ）からチャネル領域へ走行してきた電子は、ソース（Ｓ）近傍の高電界領域で加速されてアバランシェ・ブレークダウンを引き起こし、このとき発生したホットエレクトロンがサイドウォールゲート電極（ＳＷＧ）による縦方向の高電界によって窒化シリコン膜（１２５）中に注入、トラップされる。すなわち、サイドウォールゲート電極（ＳＷＧ）の直下の窒化シリコン膜（１２５）に電子がトラップされることにより、サイドウォールゲート電極（ＳＷＧ）から見たしきい値電圧が上昇する。このホットエレクトロンによる書き込み方式は、前述したフローティングゲート型メモリセルにおけるドレイン近傍のホットエレクトロンをフローティングゲートへ引き込む方式と基本的に同一である。

【００１１】また、上記メモリセルの読み出しは、ソース（１２８）を接地電位とし、サイドウォールゲート電極（１２７）と選択用ゲート電極（１２３）とに１．８Ｖの電圧を印加し、窒化シリコン膜（１２５）中の電子トラップの有無によるサイドウォールゲート電極（１２７）から見たしきい値電圧の変調をドレイン電流から判定する。このメモリセルは、ホットエレクトロンを用いて書き込みを行うために、電子をトラップさせる窒化シリコン膜（１２５）の直下の酸化シリコン膜（１２４）を前述したＭＮＯＳ型メモリセルの直接トンネル酸化膜よりも厚い膜厚（例えば１０nm程度）で形成しても書き込み速度が劣化しない。また、この酸化シリコン膜（１２４）を厚い膜厚にするほど欠陥密度が減少し、結果的にメモリセルのリテンション特性が改善する。

【００１２】ＩＥＥＥ Ｅｌｅｃｔｒｏｎ Ｄｅｖｉｃｅ Ｌｅｔｔ.,(vol.EDL-8,no.3,pp.93-95,March 1987)は、コントロールゲートを持たない単一ＭＩＳＦＥＴ構造の不揮発性メモリを開示している。この不揮発性メモリのメモリセルは、ゲート絶縁膜の上部に形成された多結晶シリコンのゲート電極と、このゲート電極の両側の半導体基板に形成されたソース、ドレインとで構成されており、ゲート絶縁膜は、２層の酸化シリコン膜の間に窒化シリコン膜を挟んだ３層構造で構成されている。

【００１３】メモリセルの書き込みは、ドレイン近傍のキャリヤを窒化シリコン膜中に注入、トラップさせることによって行う。このメモリセルは、２層の酸化シリコン膜に挟まれた窒化シリコン膜中のキャリヤがドレイン近傍の狭い領域に局在するために、ＭＮＯＳ型メモリセルに比べてリテンション特性が優れている。

【００１４】特開平６－２３２４１６号公報は、ソースとドレインとの間のチャネル領域の上部にゲート絶縁膜とキャリヤを保持するトラップ膜とが連なって形成され、このゲート絶縁膜とトラップ膜との上部にゲート電極が形成された単一ＭＩＳＦＥＴ構造の不揮発性メモリを開示している。ゲート絶縁膜は酸化シリコン膜で構成され、トラップ膜は２層の酸化シリコン膜の間に窒化シリコン膜を挟んだ３層構造で構成されている。

【００１５】メモリセルの書き込みは、トラップ膜の一部を構成する下層の酸化シリコン膜（トンネル酸化膜）を通じて電子を窒化シリコン膜注入、トラップさせることによって行う。このメモリセルは、通常のエンハンスメントＭＩＳＦＥＴのゲート絶縁膜とキャリヤを保持するメモリ部のトラップ膜とを単一ゲート電極の下部に形成するので、セル面積を縮小することができる。

【００１６】

【発明が解決しようとする課題】前述したフローティングゲート型メモリセルは、フローティングゲートの上部にコントロールゲート（ワード線）を積層することから、セル面積を比較的小さく設計することができ、大容量化に適したセル構造となっている。一方、ＭＮＯＳ型メモリセルは、フローティングゲート型メモリセルに比べてリテンション特性が優れており、信頼度の高いセル方式であると言えるが、記憶素子部と選択用とに２つの基本素子を必要とするために、同一設計ルールでのセル面積がフローティングゲート型メモリセルの４～５倍程

度大きくなり、大容量化には適さないという欠点がある。

【００１７】また、米国特許（ＵＳＰ）第５４０８１１５号に開示されたメモリセルは、フローティングゲート型メモリセルに匹敵するスケーラビリティとＭＮＯＳ型メモリセルと同等以上の高い信頼性とを有している。しかしながら、選択用ゲート電極とサイドウォールゲート電極とを有するセル構造は、フローティングゲート型メモリセルに比べて書き込み／消去動作が複雑になり、結果として必要とする周辺回路の面積が増加する。しかも、サイドウォールゲート電極の幅が１００nm程度あるため、その配線抵抗値が通常のゲート抵抗の５～７倍に増大し、これが読み出し速度の劣化を招いている。さらに、選択用ゲート電極とサイドウォールゲート電極との間、すなわち酸化シリコン膜（１２４）、窒化シリコン膜（１２５）および酸化シリコン膜（１２６）が横方向に積層された領域の直下のチャンネル領域は、その幅が３０nm程度と僅かではあるが、その上部にゲート電極が存在していない。そのため、この領域が寄生抵抗として作用し、読み出し時のドレイン電流を低下させて読み出し速度を劣化させるという問題がある。

【００１８】本発明の目的は、フローティングゲート型メモリセルに匹敵するスケーラビリティとＭＮＯＳ型メモリセルと同等以上の高い信頼性とを併せ持った新規なセル構造を備えた不揮発性メモリおよびその製造方法を提供することにある。

【００１９】本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

【００２０】

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、次のとおりである。

【００２１】本願発明の不揮発性メモリは、第１導電型の半導体基板上に形成されたゲート絶縁膜上にワード線と電気的に接続されたゲート電極が形成され、前記半導体基板内にソース、ドレインを構成する第２導電型の第１、第２半導体領域が形成され、前記第１半導体領域と前記第２半導体領域との間にチャネル領域が形成されるＭＩＳＦＥＴによって不揮発性のメモリセルが構成されており、前記ゲート絶縁膜は、少なくとも前記第１半導体領域側が第１酸化シリコン膜、窒化シリコン膜および第２酸化シリコン膜を積層した３層の絶縁膜からなる。

【００２２】前記メモリセルの書き込みは、選択したメモリセルの前記第２半導体領域を前記第１半導体領域よりも高電位にし、低不純物濃度の第２導電型半導体領域で発生したホットエレクトロンを窒化シリコン膜中の電子トラップに注入することにより行う。

【００２３】その他、本願に記載された発明の概要を項分けして説明すれば、以下の通りである。

【００２４】１．第１導電型の半導体基板上に形成されたゲート絶縁膜上にワード線と電気的に接続されたゲート電極が形成され、前記半導体基板内にソース、ドレインを構成する第２導電型の第１、第２半導体領域が形成され、前記第１半導体領域と前記第２半導体領域との間にチャネル領域が形成されるＭＩＳＦＥＴによって不揮発性のメモリセルが構成された半導体集積回路装置であって、前記ゲート絶縁膜は、少なくとも前記第１半導体領域側が第１酸化シリコン膜、窒化シリコン膜および第２酸化シリコン膜を積層した３層の絶縁膜からなり、前記メモリセルの書き込みは、前記第２半導体領域を前記第１半導体領域よりも高電位にして行うことを特徴とする半導体集積回路装置。

【００２５】２．半導体基板上に形成されたゲート絶縁膜上にワード線と電気的に接続されたゲート電極が形成され、前記半導体基板内にソース、ドレインを構成する第２導電型の第１、第２半導体領域が形成され、前記第１半導体領域と前記第２半導体領域との間にチャネル領域が形成されるＭＩＳＦＥＴによって不揮発性のメモリセルが構成された半導体集積回路装置であって、前記ゲート絶縁膜は、少なくとも前記第１半導体領域側が第１酸化シリコン膜、窒化シリコン膜および第２酸化シリコン膜を積層した３層の絶縁膜からなり、前記第１半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度は、前記第２半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度よりも低く、前記第１半導体領域側でホットエレクトロンを発生させることにより、前記窒化シリコン膜に前記ホットエレクトロンを注入することを特徴とする半導体集積回路装置。

【００２６】３．半導体基板上に形成されたゲート絶縁膜上にワード線と電気的に接続されたゲート電極が形成され、前記半導体基板内にソース、ドレインを構成する第２導電型の第１、第２半導体領域が形成され、前記第１半導体領域と前記第２半導体領域との間にチャネル領域が形成されるＭＩＳＦＥＴによって不揮発性のメモリセルが構成された半導体集積回路装置であって、前記ゲート絶縁膜は、前記第１半導体領域側が第１酸化シリコン膜、窒化シリコン膜および第２酸化シリコン膜を積層した３層の絶縁膜からなり、前記第２半導体領域側が酸化シリコン膜からなり、前記第１半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度は、前記第２半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度と異なることを特徴とする半導体集積回路装置。

【００２７】４．前記請求項１または３において、前記第１半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度は、前記第２半導体領域の前記ゲート電極の下部に延在する部分の不純物濃度よりも低いことを特徴とする半導体集積回路装置。

【００２８】５．前記請求項１、２または４において、

前記ゲート絶縁膜は、前記第１半導体領域側が前記第１酸化シリコン膜、窒化シリコン膜および第２酸化シリコン膜を積層した３層の絶縁膜からなり、前記第２半導体領域側が酸化シリコン膜からなることを特徴とする半導体集積回路装置。

【００２９】６．前記請求項１～５のいずれか一項において、前記ゲート絶縁膜は、前記第１半導体領域側と前記第２半導体領域側とがほぼ同じ電気的容量膜厚を有していることを特徴とする半導体集積回路装置。

【００３０】７．前記請求項１、２、４、５または６において、前記ゲート絶縁膜は、前記第１半導体領域側および前記第２半導体領域側が、前記第１酸化シリコン膜、窒化シリコン膜および第２酸化シリコン膜を積層した３層の絶縁膜からなることを特徴とする半導体集積回路装置。

【００３１】８．前記請求項１、３、４、５、６または７において、前記メモリセルの書き込みは、前記ゲート絶縁膜の一部を構成する前記窒化シリコン膜中にホットエレクトロンを注入して行うことを特徴とする半導体集積回路装置。

【００３２】９．前記請求項１～８のいずれか一項において、前記ゲート絶縁膜の少なくとも一部を構成する前記３層の絶縁膜のうち、前記窒化シリコン膜の下層に形成された前記第１酸化シリコン膜の膜厚は、直接トンネル電流が流れる膜厚よりも厚いことを特徴とする半導体集積回路装置。

【００３３】１０．前記請求項１～９のいずれか一項において、前記第２半導体領域は、その一端が前記ゲート電極の下部に延在する第１導電型の半導体領域と、その一端が前記ゲート電極から離間した第２導電型の半導体領域とからなり、前記第１半導体領域は、第２導電型で構成されていることを特徴とする半導体集積回路装置。

【００３４】１１．前記請求項１～１０のいずれか一項において、前記メモリセルの読み出しは、前記第１半導体領域を前記第２半導体領域よりも高電位にして行うことを特徴とする半導体集積回路装置。

【００３５】１２．前記請求項１～１０のいずれか一項において、前記メモリセルの読み出しは、前記第２半導体領域を前記第１半導体領域よりも高電位にして行うことを特徴とする半導体集積回路装置。

【００３６】１３．前記請求項１～１２のいずれか一項において、前記第１、第２半導体領域の一方の上部の絶縁膜に形成された第１接続孔に埋め込まれたプラグによってソース線が形成され、前記第１、第２半導体領域の他方の上部の前記絶縁膜に形成された第２接続孔に埋め込まれたプラグを介して、前記第１、第２半導体領域の他方にビット線が接続されていることを特徴とする半導体集積回路装置。

【００３７】１４．前記請求項１３において、前記第１接続孔および前記第２接続孔は、前記ＭＩＳＦＥＴのゲート電極のスペースに対して自己整合で形成されていることを特徴とする半導体集積回路装置。

【００３８】１５．請求項１～１４のいずれか一項において、前記メモリセルは、記憶素子部を構成する前記ＭＩＳＦＥＴと、選択用のＭＩＳＦＥＴとで構成されていることを特徴とする半導体集積回路装置。

【００３９】１６．請求項１～９、１１～１５のいずれか一項において、前記第１半導体領域と前記第２半導体領域とは同一の導電型であることを特徴とする半導体集積回路装置。

【００４０】１７．以下の工程を含むことを特徴とする半導体集積回路装置の製造方法；

（ａ）半導体基板上に第１酸化シリコン膜を形成した後、前記第１酸化シリコン膜の上部に窒化シリコン膜を形成する工程、（ｂ）前記第１酸化シリコン膜および前記窒化シリコン膜をパターニングすることにより、前記半導体基板上の第１領域に前記第１酸化シリコン膜および前記窒化シリコン膜を残し、第２領域の前記第１酸化シリコン膜および前記窒化シリコン膜を除去する工程、（ｃ）前記半導体基板上の前記第１領域の前記窒化シリコン膜の上部および前記半導体基板上の前記第２領域に第２酸化シリコン膜を形成する工程、（ｄ）前記第２酸化シリコン膜の上部に形成した導体膜をパターニングすることにより、前記第１、第２領域の前記第２酸化シリコン膜上にＭＩＳＦＥＴのゲート電極を形成する工程。

【００４１】１８．以下の工程を含むことを特徴とする半導体集積回路装置の製造方法；

（ａ）半導体基板上に第２酸化シリコン膜を形成した後、前記第２酸化シリコン膜の上部に形成した導体膜をパターニングすることにより、ＭＩＳＦＥＴのゲート電極を形成する工程、（ｂ）前記ゲート電極の上部を含む前記半導体基板上に第２窒化シリコン膜を形成した後、前記第２窒化シリコン膜の上部に第４酸化シリコン膜を形成する工程、（ｃ）前記第４酸化シリコン膜および前記第２窒化シリコン膜をエッチングすることにより、前記ＭＩＳＦＥＴの前記ゲート電極の上部および側壁を露出させる工程、（ｄ）前記第２酸化シリコン膜を等方的にエッチングすることにより、前記ゲート電極の下部の第１領域において、前記ゲート電極の下面と前記半導体基板とを露出させ、前記ゲート電極の下部の第２領域において、前記第２酸化シリコン膜を残す工程、（ｅ）前記半導体基板を熱処理することにより、前記第１領域において、前記半導体基板の表面および前記ゲート電極の下面に第１酸化シリコン膜を形成する工程、（ｆ）前記第１領域において、前記半導体基板の表面に形成された前記第１酸化シリコン膜と、前記ゲート電極の下面に形成された前記第１酸化シリコン膜との隙間を含む前記半導体基板上に第２窒化シリコン膜を形成する工程。

【００４２】１９．請求項１７または１８において、前記ゲート電極の前記第１領域側の端部に自己整合的に不

純物を導入して、前記半導体基板内に第１半導体領域を形成する工程と、前記ゲート電極の前記第２領域側の端部に自己整合的に不純物を導入して、前記半導体基板内に第２半導体領域を形成する工程とを含み、前記第１半導体領域の不純物濃度を前記第２半導体領域の不純物濃度よりも低くすることを特徴とする半導体集積回路装置の製造方法。

【００４３】２０．請求項１７、１８または１９において、前記ＭＩＳＦＥＴは不揮発性メモリを構成し、周辺回路を構成するＭＩＳＦＥＴのゲート電極と、前記不揮発性メモリを構成するＭＩＳＦＥＴのゲート電極とは、同一の導電膜をパターニングする工程で形成され、前記周辺回路を構成するＭＩＳＦＥＴのゲート絶縁膜は、前記第２酸化シリコン膜を形成する工程で形成されることを特徴とする半導体集積回路装置の製造方法。

【００４４】

【発明の実施の形態】以下、本発明の実施の形態を図面に基づいて詳細に説明する。なお、実施の形態を説明するための全図において、同一の機能を有する部材には同一の符号を付し、その繰り返しの説明は省略する。

【００４５】（実施の形態１）図１は、本発明の一実施の形態であるフラッシュメモリ（一括消去型不揮発性メモリ）の主要部を示す概略回路図である。

【００４６】このフラッシュメモリのメモリセルアレイ（ＭＡ）には、図の左右方向（Ｘ方向）に延在する複数本のワード線ＷＬ（ＷＬ1 ～ＷＬm ）および複数本のソース線ＳＬ（ＳＬ1 ～ＳＬm/2 ）、これらと直交するＹ方向に延在する複数本のビット線ＤＬ（ＤＬ1 ～ＤＬn ）および後述するＭＩＳＦＥＴ構造で構成された複数個のメモリセルＭ（M11～Mnm）が形成されている。

【００４７】上記ワード線ＷＬ（ＷＬ1 ～ＷＬm ）のそれぞれは、Ｘ方向に沿って配置された複数個のメモリセルＭのゲート電極に接続され、その一端部はロウデコーダ（Ｘ－ＤＥＣ）に接続されている。ソース線ＳＬ（ＳＬ1 ～ＳＬm/2 ）のそれぞれは、２本のワード線ＷＬの間に１本ずつ配置され、Ｙ方向に隣接する２個のメモリセルＭの共通するソースに接続されている。また、これらのソース線ＳＬ（ＳＬ1 ～ＳＬm/2 ）の一端部は、メモリセルアレイ（ＭＡ）の周辺部に配置された共通ソース線ＣＳＬに接続されている。ビット線ＤＬ（ＤＬ1 ～ＤＬn ）のそれぞれは、Ｙ方向に隣接する２個のメモリセルＭの共通するドレインに接続され、その一端部はカラムデコーダ（Ｙ－ＤＥＣ）およびセンスアンプ（ＳＡ）に接続されている。

【００４８】図２は、上記メモリセルアレイとそれに隣接する周辺回路の各一部を示す半導体基板の要部断面図、図３（Ａ）は、メモリセル約４個分の導体層パターンを示す平面図、図３（Ｂ）は、メモリセル約１２個分の導体層パターンを示す平面図である。

【００４９】ｐ型の単結晶シリコンからなる半導体基板

１のメモリセルアレイ領域にはｐ型ウエル５が形成されており、周辺回路領域にはｐ型ウエル５とｎ型ウエル６とが形成されている。また、メモリセルアレイ領域のｐ型ウエル５の下部には、このｐ型ウエル５を半導体基板１の他の領域から電気的に分離するための深いｎ型ウエル４が形成されている。ｐ型ウエル５とｎ型ウエル６のそれぞれの表面には、酸化シリコン膜で構成された素子分離用のフィールド酸化膜２が形成されている。

【００５０】メモリセルアレイ領域のｐ型ウエル５には、メモリセルを構成するｎチャネル型のＭＩＳＦＥＴＱｍが形成されている。また、周辺回路領域のｐ型ウエル５には周辺回路の一部を構成するｎチャネル型ＭＩＳＦＥＴＱｎが形成され、ｎ型ウエル６には周辺回路の他の一部を構成するｐチャネル型ＭＩＳＦＥＴＱｐが形成されている。

【００５１】メモリセルを構成するＭＩＳＦＥＴＱｍは、主としてゲート絶縁膜上に形成されたゲート電極１０ａと、一端がゲート電極１０ａの下部まで延在するｎ$^+$型半導体領域１３（ドレイン）と、ゲート電極１０ａに対してオフセットするように形成されたｎ$^+$型半導体領域１５（高濃度ソース）と、ｎ$^+$型半導体領域１５の周囲に形成され、一端がゲート電極１０ａの下部まで延在するｎ$^-$型半導体領域１１（低濃度ソース）と、これらのソース、ドレインに挟まれたチャネル形成領域（ｐ型ウエル５）とで構成されている。ゲート電極１０ａはワード線ＷＬと一体に構成され、ソース（ｎ$^+$型半導体領域１５、ｎ$^-$型半導体領域１１）はソース線ＳＬと一体に構成されている。

【００５２】ゲート電極１０ａは、例えばｎ型の多結晶シリコン膜の上部にＷ（タングステン）シリサイド膜を積層したポリサイド膜で構成され、その側壁には酸化シリコン膜で構成されたサイドウォールスペーサ１６が形成されている。また、ゲート電極１０ａの下部に形成されたゲート絶縁膜は、ドレイン側が１層の酸化シリコン膜９で構成され、ソース側が酸化シリコン膜９の下層に酸化シリコン膜７と窒化シリコン膜８とを積層した３層の絶縁膜で構成されている。

【００５３】周辺回路のｐチャネル型ＭＩＳＦＥＴＱｐは、主としてゲート絶縁膜（酸化シリコン膜９）上に形成されたゲート電極１０ｂと、ゲート電極１０ｂに対してオフセットするように形成された一対のｐ$^+$型半導体領域１４（ソース、ドレイン）と、一端がゲート電極１０ｂの下部まで延在する一対のｐ$^-$型半導体領域１２と、これらのソース、ドレインに挟まれたチャネル形成領域（ｐ型ウエル５）とで構成されている。また、周辺回路のｎチャネル型ＭＩＳＦＥＴＱｎは、主としてゲート絶縁膜（酸化シリコン膜９）上に形成されたゲート電極１０ｃと、ゲート電極１０ｃに対してオフセットするように形成された一対のｎ$^+$型半導体領域１５（ソース、ドレイン）と、一端がゲート電極１０ｃの下部まで

延在する一対のn⁻型半導体領域１１と、これらのソース、ドレインに挟まれたチャネル形成領域（p型ウエル５）とで構成されている。すなわち、周辺回路のpチャネル型ＭＩＳＦＥＴＱpおよびnチャネル型ＭＩＳＦＥＴＱnは、ＬＤＤ(Lightly Doped Drain) 構造で構成されている。pチャネル型ＭＩＳＦＥＴＱpのゲート電極１０bおよびnチャネル型ＭＩＳＦＥＴＱnのゲート電極１０cは、メモリセルのゲート電極１０aと同じくポリサイド膜で構成され、それらの側壁には酸化シリコン膜で構成されたサイドウォールスペーサ１６が形成されている。

【００５４】上記メモリセル（ＭＩＳＦＥＴＱm）、pチャネル型ＭＩＳＦＥＴＱpおよびnチャネル型ＭＩＳＦＥＴＱnの上部には厚い膜厚の酸化シリコン膜１７が形成されており、さらにその上部には例えばＡｌ合金膜で構成された配線２３～２７が形成されている。

【００５５】メモリセルアレイ領域に形成された配線２３はビット線ＤＬを構成し、酸化シリコン膜１７に形成されたコンタクトホール２０を通じてメモリセルのドレイン（n^+ 型半導体領域１３）と接続されている。また、周辺回路領域に形成された配線２４～２７のうち、配線２４、２５は、酸化シリコン膜１７に形成された一対のコンタクトホール２１を通じてpチャネル型ＭＩＳＦＥＴＱpの一対のp^+型半導体領域１４（ソース、ドレイン）と接続され、配線２６、２７は、酸化シリコン膜１７に形成された一対のコンタクトホール２２を通じてnチャネル型ＭＩＳＦＥＴＱnの一対のn^+ 型半導体領域１５（ソース、ドレイン）と接続されている。

【００５６】次に、上記フラッシュメモリのプログラム動作を図４（メモリセル約１個分を示す概略断面図）、図５（メモリセルの動作電圧表）および図６（メモリセルの書き込み動作時におけるチャネル領域の電位分布と電界強度分布とを示すグラフ）を用いて説明する。

【００５７】書き込み動作は、選択したメモリセル（ＭＩＳＦＥＴＱm）のソース（１１、１５）を接地電位（０Ｖ）とし、ゲート電極（１０a）およびドレイン（１３）にそれぞれ５Ｖの正電圧を印加する。これにより、低濃度ソース（１１）の端部に図６に示すような電界強度のピークが生じ、この領域（低濃度ソース側）で発生したホットエレクトロン（e－）が窒化シリコン膜８中の電子トラップに注入され、ゲート電極（１０a）から見たしきい値電圧が上昇することにより、書き込みが行われる。

【００５８】また、読み出し動作も同様に、選択したメモリセルのソース（１１、１５）を接地電位（０Ｖ）とし、ゲート電極（１０a）およびドレイン（１３）にそれぞれ２Ｖの正電圧を印加して行う。消去動作は、メモリセルのドレイン（１３）を接地電位（０Ｖ）とし、ソース（１１、１５）に５Ｖの正電圧、ゲート電極（１０a）に－１０Ｖの負電圧をそれぞれ印加し、窒化シリコン膜８中にトラップされた電子を基板（p型ウエル５）側へ放出することにより、ゲート電極（１０a）から見たしきい値電圧を下降させて行う。

【００５９】次に、上記不揮発性メモリの製造方法の一例を図７～図１８（メモリセルアレイ領域とそれに隣接する周辺回路領域の各一部を示す半導体基板の要部断面図）を用いて説明する。

【００６０】まず、図７に示すように、１０Ωcm程度の比抵抗を有するp型の単結晶シリコンからなる半導体基板１を用意し、その表面に選択酸化（ＬＯＣＯＳ）法で膜厚５００nm程度のフィールド酸化膜２を形成した後、半導体基板１を熱酸化することにより、上記フィールド酸化膜２で囲まれた素子形成領域の表面に膜厚２０nm程度の酸化シリコン膜３を形成する。酸化シリコン膜３は、次の工程で半導体基板１に不純物をイオン打ち込みする際のマスクとして使用される。

【００６１】次に、図８に示すように、メモリセルアレイ領域の半導体基板１に深いn型ウエル４を形成した後、メモリセルアレイ領域および周辺回路の一部（nチャネル型ＭＩＳＦＥＴ形成領域）の半導体基板１に浅いp型ウエル５を形成し、周辺回路の他の一部（pチャネル型ＭＩＳＦＥＴ形成領域）の半導体基板１に浅いn型ウエル６を形成する。

【００６２】深いn型ウエル４は、メモリセルアレイ領域に開孔部を設けた膜厚５μm程度のフォトレジスト膜をマスクにして、加速エネルギー３０００ｋｅＶ、ドーズ量$1\times10^{13}/cm^2$の条件で半導体基板１にn型不純物（リン）をイオン打ち込みして形成する。また、浅いp型ウエル５は、メモリセルアレイ領域とnチャネル型ＭＩＳＦＥＴ形成領域とに開孔部を設けた膜厚２．５μm程度のフォトレジスト膜をマスクにして、加速エネルギー４５０ｋｅＶ、ドーズ量$1\times10^{13}/cm^2$および加速エネルギー２００ｋｅＶ、ドーズ量$3\times10^{12}/cm^2$の条件で半導体基板１にp型不純物（ホウ素）をイオン打ち込みして形成する。さらに、浅いn型ウエル６は、pチャネル型ＭＩＳＦＥＴ形成領域に開孔部を設けた膜厚２．５μm程度のフォトレジスト膜をマスクにして、加速エネルギー１０００ｋｅＶ、ドーズ量$1.5\times10^{13}/cm^2$、加速エネルギー３７０ｋｅＶ、ドーズ量$3\times10^{13}/cm^2$および加速エネルギー１８０ｋｅＶ、ドーズ量$1\times10^{12}/cm^2$の条件で半導体基板１にn型不純物（リン）をイオン打ち込みして形成する。

【００６３】なお、上記したp型ウエル５を形成するためのイオン打ち込み工程で、メモリセル（ＭＩＳＦＥＴＱm）およびnチャネル型ＭＩＳＦＥＴＱnのしきい値電圧（Vth）を調整するための不純物（ホウ素）を同時にイオン注入する（加速エネルギー５０ｋｅＶ、ドーズ量$1.2\times10^{12}/cm^2$）。また、n型ウエル６を形成するためのイオン打ち込み工程で、pチャネル型ＭＩＳＦＥＴＱpのしきい値電圧（Vth）を調整するための不純

物（ホウ素）を同時にイオン注入する（加速エネルギー２０ｋｅＶ、ドーズ量１．５×$10^{12}/cm^2$）。

【００６４】次に、ｐ型ウエル５、ｎ型ウエル６のそれぞれの表面の酸化シリコン膜３をウェットエッチングで除去した後、図９に示すように、半導体基板１を７５０℃程度で熱酸化してｐ型ウエル５、ｎ型ウエル６のそれぞれの表面に膜厚７nm程度の酸化シリコン膜７を形成し、さらに酸化シリコン膜７の上部に８００℃程度の熱ＣＶＤ法で膜厚７nm程度の窒化シリコン膜８を堆積する。

【００６５】次に、図１０に示すように、上記窒化シリコン膜８と酸化シリコン膜７とをパターニングして、メモリセルのソース形成領域とその近傍のみにこれらの膜を残す。窒化シリコン膜８のパターニングは、上記ソース形成領域とその近傍とに開孔部を設けた膜厚１μｍ程度のフォトレジスト膜をマスクにしたドライエッチングで行い、酸化シリコン膜７のパターニングは、上記フォトレジスト膜をアッシングで除去した後、窒化シリコン膜８をマスクにしたドライエッチングで行う。ソース形成領域とその近傍に残す上記２層の絶縁膜（酸化シリコン膜７、窒化シリコン膜８）は、後の工程で形成されるゲート電極１０ａの下部に位置する部分の長さ（ゲート長方向の長さ）が２０nm～２００nm程度となるようにその幅を調整する。

【００６６】次に、図１１に示すように、半導体基板１を８００℃程度で熱酸化してｐ型ウエル５、ｎ型ウエル６のそれぞれの表面に膜厚１５nm程度の酸化シリコン膜９を形成する。このとき、メモリセルアレイ領域の窒化シリコン膜８も同時に酸化されるので、その表面にも膜厚２nm程度の酸化シリコン膜９が形成される。

【００６７】次に、図１２に示すように、メモリセルアレイ領域の酸化シリコン膜９上にメモリセル（ＭＩＳＦＥＴＱｍ）のゲート電極１０ａを形成し、周辺回路領域の酸化シリコン膜９上にｐチャネル型ＭＩＳＦＥＴＱｎのゲート電極１０ｂとｎチャネル型ＭＩＳＦＥＴＱｐのゲート電極１０ｃとを形成する。ゲート電極１０ａ、１０ｂ、１０ｃは、酸化シリコン膜９上に６００℃程度の熱ＣＶＤ法で膜厚１００nm程度、リン濃度２×$10^{20}/cm^3$程度の多結晶シリコン膜と膜厚５０nm程度のＷシリサイド膜とを堆積した後、フォトレジスト膜をマスクにしたドライエッチングでこれらの膜をパターニングして形成する。

【００６８】次に、図１３に示すように、半導体基板１の全面に加速エネルギー４０ｋｅＶ、ドーズ量１×$10^{13}/cm^2$の条件でｎ型不純物（リン）をイオン打ち込みすることにより、ゲート電極１０ａ、１０ｃのそれぞれの両側のｐ型ウエル５およびゲート電極１０ｂの両側のｎ型ウエル６に低不純物濃度のn^-型半導体領域１１を形成する。

【００６９】次に、図１４に示すように、メモリセルの

ドレイン形成領域に開孔部を設けた膜厚１μｍ程度のフォトレジスト膜をマスクにして、加速エネルギー５０ｋｅＶ、ドーズ量３×$10^{15}/cm^2$の条件でｐ型ウエル５にｎ型不純物（ヒ素）をイオン打ち込みすることにより、メモリセルのドレインを構成するn^+型半導体領域１３を形成する。

【００７０】次に、図１５に示すように、ｐチャネル型ＭＩＳＦＥＴ形成領域に開孔部を設けた膜厚１μｍ程度のフォトレジスト膜をマスクにして、加速エネルギー５０ｋｅＶ、ドーズ量２×$10^{13}/cm^2$の条件でｎ型ウエル６にｐ型不純物（二フッ化ホウ素）をイオン打ち込みすることにより、ゲート電極１０ｂの両側のｎ型ウエル６に前記n^-型半導体領域１１を補償して低不純物濃度のp^-型半導体領域１２を形成する。

【００７１】次に、図１６に示すように、半導体基板１上にＣＶＤ法で膜厚２００nm程度の酸化シリコン膜（図示せず）を堆積した後、この酸化シリコン膜を異方性エッチングすることにより、ゲート電極１０ａ、１０ｂ、１０ｃのそれぞれの側壁に幅１５０nm程度のサイドウォールスペーサ１６を形成する。このとき、メモリセルのソース形成領域を覆っている酸化シリコン膜９と窒化シリコン膜８も同時にエッチングされる。

【００７２】次に、図１７に示すように、ｐチャネル型ＭＩＳＦＥＴ形成領域に開孔部を設けた膜厚１μｍ程度のフォトレジスト膜をマスクにして、加速エネルギー５０ｋｅＶ、ドーズ量３×$10^{15}/cm^2$の条件でｎ型ウエル６にｐ型不純物（二フッ化ホウ素）をイオン打ち込みすることにより、ｐチャネル型ＭＩＳＦＥＴのソース、ドレインを構成する高不純物濃度のp^+型半導体領域１４を形成する。

【００７３】続いて、メモリセルのソース形成領域とｎチャネル型ＭＩＳＦＥＴ形成領域とに開孔部を設けた膜厚１μｍ程度のフォトレジスト膜をマスクにして、加速エネルギー５０ｋｅＶ、ドーズ量２×$10^{15}/cm^2$の条件でｐ型ウエル５にｎ型不純物（ヒ素）をイオン打ち込みすることにより、メモリセルのソースを構成する高不純物濃度のn^+型半導体領域１５と、ｎチャネル型ＭＩＳＦＥＴのソース、ドレインを構成する高不純物濃度のn^+型半導体領域１５とを形成する。ここまでの工程で、メモリセル（ＭＩＳＦＥＴＱｍ）と周辺回路のＭＩＳＦＥＴ（ｎチャネル型ＭＩＳＦＥＴＱｎ、ｐチャネル型ＭＩＳＦＥＴＱｐ）とが完成する。

【００７４】次に、図１８に示すように、半導体基板１上にＣＶＤ法で膜厚５００nm程度の酸化シリコン膜１７を堆積した後、フォトレジスト膜をマスクにして酸化シリコン膜１７をドライエッチングすることにより、メモリセルのドレインの上部、ｎチャネル型ＭＩＳＦＥＴＱｎのソース、ドレインの上部およびｐチャネル型ＭＩＳＦＥＴＱｐのソース、ドレインの上部にそれぞれコンタクトホール２０、２１、２２を形成する。

【００７５】その後、コンタクトホール２０～２２の内部を含む酸化シリコン膜１７上にスパッタリング法で膜厚５００nm程度のＡｌ合金膜を堆積し、フォトレジスト膜をマスクにしたドライエッチングでこのＡｌ合金膜をパターニングして配線２３～２７を形成することにより、前記図２に示す本実施の形態のフラッシュメモリが略完成する。

【００７６】上記のように構成された本実施の形態のフラッシュメモリは、従来のフローティングゲート型メモリセルと同様、メモリセルが単一のＭＩＳＦＥＴで構成されているために、書き込み／消去動作を比較的簡便に行うことができ、必要とする周辺回路の面積を増加させることがない。また、製造工程も簡略になる。

【００７７】本実施の形態のフラッシュメモリは、読み出し動作の際に、従来のサイドウォールゲート電極を備えたメモリセルのような高抵抗配線を用いないので、読み出し速度の劣化が発生しない。また、書き込み動作の際には、ゲート電極とドレインとに正電圧を印加し、ソース近傍で発生させたホットエレクトロンを窒化シリコン膜中の電子トラップに注入する方式を採用するため、接地電位のソースとゲート電極間の電位差が大きくなることによって注入効率が向上し、従来のセル構造に比べてより低電圧動作が可能となる。

【００７８】本実施の形態のフラッシュメモリは、メモリセルのゲート電極がチャネル領域の全面を覆っているために、従来のサイドウォールゲート電極を備えたセル構造で問題となるサイドウォールゲート電極－制御ゲート電極間の絶縁膜直下における寄生抵抗の発生がなく、読み出し動作時のドレイン電流の低下を招くことがない。

【００７９】本実施の形態のフラッシュメモリの製造方法は、メモリセルのソース側のゲート絶縁膜（酸化シリコン膜７、窒化シリコン膜８、酸化シリコン膜９からなる３層の絶縁膜）をゲート電極に対して自己整合（セルフアライン）で形成するので、従来のフローティングゲート型メモリセルと同等のセル面積に設計することができ、スケーラビリティに優れた不揮発性メモリを実現することができる。

【００８０】（実施の形態２）本実施の形態のフラッシュメモリの製造方法を図１９～図３３（メモリセルアレイ領域とそれに隣接する周辺回路領域の各一部を示す半導体基板の要部断面図）を用いて説明する。

【００８１】まず、図１９に示すように、ｐ型の単結晶シリコンからなる半導体基板１の表面にフィールド酸化膜２を形成した後、フィールド酸化膜２で囲まれた素子形成領域の表面に酸化シリコン膜３を形成する。続いて、メモリセルアレイ領域の半導体基板１に深いｎ型ウエル４を形成した後、メモリセルアレイ領域および周辺回路の一部（ｎチャネル型ＭＩＳＦＥＴ形成領域）の半導体基板１に浅いｐ型ウエル５を形成し、周辺回路の他

の一部（ｐチャネル型ＭＩＳＦＥＴ形成領域）の半導体基板１に浅いｎ型ウエル６を形成する。ここまでの工程は、前記実施の形態１と同じである。

【００８２】次に、図２０に示すように、半導体基板１を８００℃程度で熱酸化してｐ型ウエル５、ｎ型ウエル６のそれぞれの表面に膜厚１５nm程度のゲート酸化膜３０を形成した後、図２１に示すように、半導体基板１上に６００℃程度の熱ＣＶＤ法で多結晶シリコン膜（図示せず）を膜厚２００程度堆積した後、フォトレジスト膜をマスクにしてこの多結晶シリコン膜３１をドライエッチングすることにより、メモリセルのゲート電極３１ａおよび周辺回路のゲート電極３１ｂ、３１ｃを形成する。

【００８３】次に、図２２に示すように、上記ゲート電極３１ａ、３１ｂ、３１ｃの上部を含む半導体基板１上にＣＶＤ法で膜厚２０nm程度の窒化シリコン膜３２を堆積した後、窒化シリコン膜３２の上部にＣＶＤ法で膜厚５０nm程度の酸化シリコン膜３３を堆積する。

【００８４】次に、図２３に示すように、メモリセルのソース形成領域とその近傍に開孔部を設けた膜厚１μm程度のフォトレジスト膜をマスクにして酸化シリコン膜３３をウェットエッチングし、続いて上記フォトレジスト膜をアッシングで除去した後、酸化シリコン膜３３をマスクにして窒化シリコン膜３２をウェットエッチングすることにより、メモリセルのソース形成領域とその近傍のゲート電極３１ａとを覆っている窒化シリコン膜３２を除去する。

【００８５】次に、図２４に示すように、上記窒化シリコン膜３２をマスクにしたウェットエッチングでメモリセルのソース形成領域を覆っているゲート酸化膜３０を除去する。このとき、ソース形成領域に隣接してパターン形成されたゲート電極３１ａの下部のゲート酸化膜３０もエッチングされ、その一部が端部から幅７０nm程度にわたって除去（アンダーカット）される。

【００８６】次に、図２５に示すように、半導体基板１を７５０℃程度で熱酸化してメモリセルのソース形成領域とその近傍に露出したｐ型ウエル５の表面に膜厚５nm程度の酸化シリコン膜３４を形成する。このとき、メモリセルのソース形成領域の近傍に露出しているゲート電極３１ａも同時に酸化され、その表面に膜厚５nm程度の酸化シリコン膜３５が形成される。

【００８７】次に、図２６に示すように、半導体基板１上にＣＶＤ法で膜厚１０nm程度の窒化シリコン膜３６を堆積する。これにより、ゲート電極１０ａの下部のソース形成領域側に酸化シリコン膜３４、窒化シリコン膜３６および酸化シリコン膜３５からなる３層のゲート絶縁膜が形成される。

【００８８】次に、図２７に示すように、半導体基板１の全面に加速エネルギー４０ｋｅＶ、ドーズ量$1\times10^{13}/cm^2$の条件でｎ型不純物（リン）をイオン打ち込みす

ることにより、ゲート電極１０ａ、１０ｃのそれぞれの両側のｐ型ウエル５およびゲート電極１０ｂの両側のｎ型ウエル６に低不純物濃度のｎ$^-$型半導体領域３７を形成する。

【００８９】次に、図２８に示すように、メモリセルのドレイン形成領域に開孔部を設けた膜厚１μｍ程度のフォトレジスト膜をマスクにして、加速エネルギー５０ｋｅＶ、ドーズ量３×１０^{15}/cm^{2}の条件でｐ型ウエル５にｎ型不純物（ヒ素）をイオン打ち込みすることにより、メモリセルのドレインを構成するｎ$^+$型半導体領域３９を形成する。

【００９０】次に、図２９に示すように、ｐチャネル型ＭＩＳＦＥＴ形成領域に開孔部を設けた膜厚１μｍ程度のフォトレジスト膜をマスクにして、加速エネルギー５０ｋｅＶ、ドーズ量２×１０^{13}/cm^{2}の条件でｎ型ウエル６にｐ型不純物（二フッ化ホウ素）をイオン打ち込みすることにより、ゲート電極３１ｂの両側のｎ型ウエル６に前記ｎ$^-$型半導体領域３７を補償して低不純物濃度のｐ$^-$型半導体領域３８を形成する。

【００９１】次に、図３０に示すように、半導体基板１上にＣＶＤ法で膜厚２００nm程度の窒化シリコン膜を堆積した後、この窒化シリコン膜を異方性エッチングすることにより、ゲート電極３１ａ、３１ｂ、３１ｃのそれぞれの側壁に幅１５０nm程度のサイドウォールスペーサ４２を形成する。このとき、ゲート電極３１ａ、３１ｂ、３１ｃの上部を覆っている酸化シリコン膜３５および窒化シリコン膜３５も同時にエッチングされ、ゲート電極３１ａ、３１ｂ、３１ｃの表面が露出する。

【００９２】次に、図３１に示すように、ｐチャネル型ＭＩＳＦＥＴ形成領域に開孔部を設けた膜厚１μｍ程度のフォトレジスト膜をマスクにして、加速エネルギー５０ｋｅＶ、ドーズ量３×１０^{15}/cm^{2}の条件でｎ型ウエル６にｐ型不純物（二フッ化ホウ素）をイオン打ち込みすることにより、ｐチャネル型ＭＩＳＦＥＴのソース、ドレインを構成する高不純物濃度のｐ$^+$型半導体領域４０を形成する。

【００９３】続いて、メモリセルのソース形成領域とｎチャネル型ＭＩＳＦＥＴ形成領域とに開孔部を設けた膜厚１μｍ程度のフォトレジスト膜をマスクにして、加速エネルギー５０ｋｅＶ、ドーズ量２×１０^{15}/cm^{2}の条件でｐ型ウエル５にｎ型不純物（ヒ素）をイオン打ち込みすることにより、メモリセルのソースを構成する高不純物濃度のｎ$^+$型半導体領域４１と、ｎチャネル型ＭＩＳＦＥＴのソース、ドレインを構成する高不純物濃度のｎ$^+$型半導体領域４１とを形成する。ここまでの工程で、メモリセル（ＭＩＳＦＥＴＱｍ）と周辺回路のＭＩＳＦＥＴ（ｎチャネル型ＭＩＳＦＥＴＱｎ、ｐチャネル型ＭＩＳＦＥＴＱｐ）とが完成する。

【００９４】次に、半導体基板１の表面をウェットエッチングしてそれぞれのＭＩＳＦＥＴのソース、ドレイン

の表面を覆っている酸化シリコン膜３４を除去した後、図３２に示すように、ゲート電極３１ａ、３１ｂ、３１ｃおよびソース、ドレイン（ｎ$^+$型半導体領域３９、ｐ$^+$型半導体領域４０、ｎ$^+$型半導体領域４１）の表面に低抵抗のシリサイド層４３を形成する。シリサイド層４３は、例えば半導体基板１上にスパッタリング法でＣｏ（コバルト）膜、Ｔｉ（コバルト）膜などの高融点金属膜を堆積し、次いで半導体基板１を熱処理して高融点金属膜と基板（Ｓｉ）およびゲート電極（３１ａ～３１ｃ）とを反応させてＣｏシリサイド層を形成した後、未反応の高融点金属膜をウェットエッチングで除去することにより形成する。

【００９５】次に、図３３に示すように、前記実施の形態１と同様の方法により、半導体基板１上に堆積した酸化シリコン膜４４にコンタクトホール４５、４６、４７を形成した後、酸化シリコン膜４４の上部に配線４８～５２を形成することにより、本実施の形態２のフラッシュメモリが略完成する。

【００９６】図３４は、上記した製造方法で使用するフォトマスクの一覧表である。全工程で使用する１３枚のフォトマスクのうち、メモリセルの製造に固有のフォトマスクは窒化シリコン膜の加工用（No. ６）とドレイン形成用（No. ７）の２枚であり、非常に簡略化されている。

【００９７】また、上記した方法で製造したフラッシュメモリの書き込み／消去動作特性およびリテンション特性は、前記実施の形態１のフラッシュメモリと同程度であった。

【００９８】（実施の形態３）図３５は、本実施の形態のフラッシュメモリのセル構造を示す半導体基板の要部断面図である。

【００９９】前記実施の形態１のメモリセル（ＭＩＳＦＥＴＱｍ）は、ドレイン側のゲート絶縁膜を１層の酸化シリコン膜９で構成しているのに対し、本実施の形態では、ドレイン側のゲート絶縁膜を酸化シリコン膜９およびその下層に形成した酸化シリコン膜６０の２層膜で構成している。また、これら２層の酸化シリコン膜９、６０で構成されたドレイン側のゲート絶縁膜の電気的容量膜厚は、酸化シリコン膜７、９とそれらに挟まれた窒化シリコン膜８とで構成されたソース側のゲート絶縁膜の電気的容量膜厚にほぼ等しい。すなわち、このメモリセルのゲート絶縁膜は、ドレイン側とソース側とがほぼ等しい電気的容量膜厚（例えば１７．５nm程度）で構成されている。

【０１００】本実施の形態のメモリセルの上記した以外の構成およびプログラム動作は、前記実施の形態１のメモリセルと同じである。また、本実施の形態のメモリセルの製造方法は、半導体基板１を熱処理して酸化シリコン膜６０を形成する工程が一工程増える以外は、前記実施の形態１の製造方法と同じである。

【０１０１】本実施の形態のフラッシュメモリによれば、ゲート絶縁膜の電気的容量膜厚をゲート電極１０ａの下部全体でほぼ同じにしたことにより、ソース側のゲート絶縁膜（酸化シリコン膜９、窒化シリコン膜８、酸化シリコン膜７）のゲート長方向に沿った長さが製造プロセスのばらつきによって変動した場合でも、ドレイン電流の駆動能力が変動することがない。これにより、書き込み動作時のドレイン電流が一定となるので、書き込み時間の変動が防止され、安定なメモリセル特性を得ることが可能となる。

【０１０２】（実施の形態４）図３６は、本実施の形態のフラッシュメモリのセル構造を示す半導体基板の要部断面図である。

【０１０３】前記実施の形態１のメモリセルは、ソース側のゲート絶縁膜のみを３層膜（酸化シリコン膜９、窒化シリコン膜８、酸化シリコン膜７）で構成しているのに対し、本実施の形態では、ゲート電極１０ａの下部のゲート絶縁膜全体を上記３層膜（酸化シリコン膜９、窒化シリコン膜８、酸化シリコン膜７）で構成している。これら３層膜の膜厚は、いずれも７nm程度である。

【０１０４】本実施の形態のメモリセルの上記した以外の構成およびプログラム動作は、前記実施の形態１のメモリセルと同じである。また、本実施の形態のメモリセルの製造方法は、酸化シリコン膜７と窒化シリコン膜８とをパターニングしてソース側のみに残す工程が一工程省略される以外は、前記実施の形態１の製造方法と同じである。このメモリセルの書き込みは、１μ秒であった。

【０１０５】（実施の形態５）図３７は、本実施の形態のフラッシュメモリのセル構造を示す半導体基板の要部断面図である。

【０１０６】このフラッシュメモリは、記憶素子部であるＭＩＳＦＥＴＱｃと選択用ＭＩＳＦＥＴＱｓとでメモリセルを構成している。記憶素子部のＭＩＳＦＥＴＱｃは、主として膜厚８nm程度の下部ゲート酸化膜７０と、膜厚１０nm程度の窒化シリコン膜７１と、膜厚１０nm程度の上部ゲート酸化膜７２とからなる３層構造のゲート絶縁膜上に形成された多結晶シリコン膜などからなる書き込み／消去用のゲート電極（ＰＥＧ）７３と、このゲート電極７３の両側の半導体基板１に形成されたソース、ドレイン（接続拡散層）とで構成されている。

【０１０７】ソースは、一端部がゲート電極７３の下部まで延在する低不純物濃度のn^-型半導体領域７４と、ゲート電極７３に対してオフセットするように形成された高不純物濃度のn^+型半導体領域７５とで構成されており、ドレイン（接続拡散層）は、一端部がゲート電極７３の下部まで延在する高不純物濃度のn^+型半導体領域７６で構成されている。

【０１０８】また、選択用ＭＩＳＦＥＴＱｓは、主として厚さ４nm程度のゲート酸化膜７７の上部に形成された多結晶シリコン膜などからなる選択用のゲート電極（ＳＧ）７８と、このゲート電極７８の両側の半導体基板１に形成されたソース（接続拡散層）、ドレインとで構成されている。ドレインは、一端部がゲート電極７８の下部まで延在する高不純物濃度のn^+型半導体領域７９で構成されている。ソースは、上記ＭＩＳＦＥＴＱｃのドレインである高不純物濃度のn^+型半導体領域７６で構成され、その一端部はゲート電極７８の下部まで延在している。

【０１０９】上記フラッシュメモリのプログラム動作を図３８（メモリセルの動作電圧表）を用いて説明する。書き込みは、選択用ＭＩＳＦＥＴＱｓのドレインに５Ｖ、ゲート電極７８に２Ｖを印加して選択用ＭＩＳＦＥＴＱｓをオン（ＯＮ）にし、記憶素子部のＭＩＳＦＥＴＱｃのソースを接地電位（０Ｖ）とし、ゲート電極７３に５Ｖを印加することにより、ソースの一部を構成する低不純物濃度のn^-型半導体領域７４の近傍に電界強度のピークを生じさせる。これにより、この領域で発生したホットエレクトロンが窒化シリコン膜７１中の電子トラップに注入され、ＭＩＳＦＥＴＱｃのゲート電極７３から見たしきい値電圧が４Ｖ以上に上昇することによって書き込みが行われる。このメモリセルは、ゲート電極７３に印加する電圧でドレイン電流を抑制することができるので、基板および書き込み／消去用のゲート電極の電位を制御し、直接トンネル酸化膜を介して基板側から窒化シリコン膜中へ電子を全面注入する従来のＭＮＯＳ型メモリセルに比べると、より低い消費電力で書き込みを行うことができる。

【０１１０】消去動作は、ＭＩＳＦＥＴＱｃのゲート電極７３に－１０Ｖ、ソースとウエルとに５Ｖを印加し、窒化シリコン膜７１中の電子を放出することによって行う。また、読み出し動作は、選択用ＭＩＳＦＥＴＱｓのドレインおよびゲート電極７８と、ＭＩＳＦＥＴＱｃのゲート電極７３とに２Ｖを印加し、ＭＩＳＦＥＴＱｃのしきい値電圧を判定することによって行う。

【０１１１】（実施の形態６）図３９は、本実施の形態のフラッシュメモリのセル構造を示す半導体基板の要部断面図である。

【０１１２】このメモリセルを構成するＭＩＳＦＥＴは、主としてゲート絶縁膜上に形成された多結晶シリコン膜などからなるゲート電極８３と、このゲート電極８３の両側の半導体基板１に形成されたソース、ドレインとで構成されている。ソースは、一端部がゲート電極８３の下部まで延在する高不純物濃度のn^+型半導体領域８４で構成されており、ドレインは、一端部がゲート電極８３の下部まで延在する低不純物濃度（1×10^{18}～$10^{19}/cm^3$程度）のp^-型半導体領域８５と、ゲート電極８３に対してオフセットするように形成された高不純物濃度のn^+型半導体領域８６とで構成されている。また、ゲート絶縁膜は、ソース側が膜厚１０nm程度のゲー

ト酸化膜８２で構成されているのに対し、ドレイン側が膜厚８nm程度の下部ゲート酸化膜８０と、膜厚１０nm程度の窒化シリコン膜８１と、膜厚１０nm程度の上部ゲート酸化膜８２とで構成されている。このように、本実施の形態のメモリセルは、書き込み時のホットエレクトロン注入をドレイン側で行う点に特徴がある。

【０１１３】図４０に示すように、このフラッシュメモリの読み出しおよび消去動作は、前記実施の形態１のメモリセルと同じである。一方、書き込みは、選択したメモリセルのドレインを接地電位（０Ｖ）とし、ゲート電極８３およびソースにそれぞれ５Ｖの正電圧を印加して行う。

【０１１４】図４１は、書き込み動作時における各端子への電圧印加の時間変化を示すグラフである。書き込みは、まず選択したメモリブロックの共通ソース線を５Ｖに充電した後、全ビット線を５Ｖへプリチャージする。次に、選択したワード線のみを５Ｖに昇圧した後、選択したビット線のみを０Ｖに降下させる。この０Ｖに降下させた時間が書き込み時間であり、この時間内に選択したメモリセルのソースからドレイン方向へチャネル電流が流れる。このとき、図４２に示すように、ソース側５Ｖ、ドレイン側０Ｖに設定された電位の大半は、低濃度ドレイン（p^-型半導体領域８５）領域で降下するために、ドレイン端部に電界強度のピークが生じる。そして、この高電界によって発生したホットエレクトロンが、選択したワード線に印加された５Ｖの縦方向電界によって加速され、窒化シリコン膜８１中の電子トラップに注入されることにより、書き込みが行われる。

【０１１５】（実施の形態７）図４３は、本実施の形態のフラッシュメモリのセル構造を示す半導体基板の要部断面図である。

【０１１６】このメモリセルは、書き込み時のホットエレクトロン注入をドレイン側で行うもので、一端部がゲート電極８３の下部まで延在する低不純物濃度のn^-型半導体領域８７と、ゲート電極８３に対してオフセットするように形成された高不純物濃度のn^+型半導体領域８４とでソースが構成されている以外は、前記実施の形態６と同一のセル構造を有している。

【０１１７】書き込みは、前記実施の形態６と同様、選択したメモリブロックの共通ソース線を５Ｖに充電した後、全ビット線を５Ｖへプリチャージすることにより開始される。ところで、この書き込み用の５Ｖ電源が、チップ上に形成された昇圧回路のような内部電源である場合は、電源の供給能力が限られるために、充電される共通ソース線の接合リーク電流が大きいと、十分な電圧に充電できないという問題が生じる。本実施の形態では、ソース側に低不純物濃度のn^-型半導体領域８７を形成したことにより、書き込み時にソースを充電する際、ソース接合の電界が緩和され、ソース接合のリーク電流低減および接合耐圧の向上が図られるので、上記のような

問題を回避することができる。

【０１１８】（実施の形態８）図４４は、本実施の形態のフラッシュメモリのセル構造を示す要部平面図、図４５は、図４４のＡ－Ａ’線に沿った半導体基板の要部断面図である。

【０１１９】本実施の形態のメモリセルを構成するＭＩＳＦＥＴＱｍは、前記実施の形態１と同様、ソース側のゲート絶縁膜を３層膜（酸化シリコン膜９、窒化シリコン膜８、酸化シリコン膜７）で構成し、ドレイン側を１層の酸化シリコン膜９で構成している。一方、ビット線ＤＬとドレイン（n^+型半導体領域９２）とは、ドレインの上部に形成したプラグ９８を介して電気的に接続されている。また、ゲート電極９０の延在方向に沿った複数のメモリセルのソース（n^+型半導体領域９２）は、その上部に形成したプラグ９８によって構成されたソース線（ＳＬ）を介して電気的に接続されている。

【０１２０】上記メモリセルを製造するには、まず図４６に示すように、前記実施の形態１と同様の方法でｐ型の半導体基板１に深いｎ型ウエル４と浅いｐ型ウエル５とを形成した後、ｐ型ウエル５の表面に、ソース側が３層膜（酸化シリコン膜９、窒化シリコン膜８、酸化シリコン膜７）で構成され、ドレイン側が１層の酸化シリコン膜９で構成されたゲート絶縁膜を形成する。

【０１２１】上記酸化シリコン膜７は、半導体基板１を８００℃程度で熱酸化して形成し、その膜厚は１１nm程度とする。また、窒化シリコン膜８は７３０℃程度の熱ＣＶＤ法で形成し、その膜厚は１０nm程度とする。さらに、酸化シリコン膜９は上記窒化シリコン膜８と酸化シリコン膜７とをパターニングして、メモリセルのソース形成領域とその近傍のみにこれらの膜を残した後、半導体基板１を８００℃程度で熱酸化して形成し、その膜厚は１５nm程度とする。

【０１２２】次に、図４７に示すように、酸化シリコン膜９の上部にＣＶＤ法で膜厚１００nm程度、リン濃度２×$10^{20}/cm^3$程度の多結晶シリコン膜を堆積し、次いでその上部にＣＶＤ法で膜厚２００nm程度の窒化シリコン膜９３を堆積した後、フォトレジスト膜をマスクにしたドライエッチングでこれらの膜をパターニングすることにより、上記多結晶シリコン膜で構成されたゲート電極９０を形成する。

【０１２３】次に、図４８に示すように、ソース形成領域に開孔部を設けたフォトレジスト膜をマスクにして、加速エネルギー２０ｋｅＶ、ドーズ量１×$10^{13}/cm^2$の条件で斜め３０度の方向からｐ型ウエル５にｐ型不純物（ホウ素）をイオン打ち込みすることにより、p^-型半導体領域９１を形成する。続いて、メモリセルアレイ領域の全面に加速エネルギー５０ｋｅＶ、ドーズ量２×$10^{15}/cm^2$の条件でｎ型不純物（ヒ素）をイオン打ち込みすることにより、ゲート電極９０の両側のｐ型ウエル５にソース、ドレインを構成するn^+型半導体領域９２を

形成する。

【０１２４】次に、図４９に示すように、半導体基板１上にＣＶＤ法で窒化シリコン膜（を堆積した後、この窒化シリコン膜を異方性エッチングすることにより、ゲート電極９０の側壁にサイドウォールスペーサ９４を形成する。このとき、ソース、ドレインの表面を覆っているゲート絶縁膜も同時にエッチングされる。

【０１２５】次に、図５０に示すように、半導体基板１上にＣＶＤ法で酸化シリコン膜９５を堆積した後、ソース、ドレインの上部に開孔部を設けたフォトレジスト膜をマスクにして、この酸化シリコン膜９５をエッチングすることにより、ソースの上部を含むソース線形成領域にコンタクトホール９６を形成し、ドレインの上部にコンタクトホール９７を形成する。

【０１２６】上記酸化シリコン膜９５をエッチングする工程では、ゲート電極９０の側壁に形成された窒化シリコンのサイドウォールスペーサ９４がエッチングストッパとして機能するので、上記コンタクトホール９６、９７は、ゲート電極９０のスペースに対して自己整合（セルフアライン）で形成される。これにより、コンタクトホール９６、９７とゲート電極９０との合わせ余裕が不要となるので、ゲート電極９０のスペースを最小加工寸法で設計することができる。

【０１２７】次に、図５１に示すように、コンタクトホール９６の内部にソース線（ＳＬ）を形成し、コンタクトホール９７の内部にプラグ９８を形成する。ソース線（ＳＬ）およびプラグ９８は、酸化シリコン膜９５の上部にｎ型不純物をドープした多結晶シリコン膜をＣＶＤ法で堆積した後、この多結晶シリコン膜の表面を化学的機械的研磨（ＣＭＰ）法で平坦化することにより形成する。

【０１２８】その後、酸化シリコン膜９５の上部にＣＶＤ法で酸化シリコン膜９９を堆積した後、酸化シリコン膜９９の上部にスパッタリング法でＡｌ合金膜を堆積し、フォトレジスト膜をマスクにしたドライエッチングでこのＡｌ合金膜をパターニングしてビット線ＤＬを形成することにより、前記図４４および図４５に示す本実施の形態のフラッシュメモリが略完成する。

【０１２９】本実施の形態によれば、ゲート電極９０のスペースを最小加工寸法で設計することができるので、ゲート長０．３μｍでセル面積を０．５μｍ×０．４μｍ＝０．２μｍ^{2}まで縮小することができた。また、メモリセルの書き込み時間は５マイクロ秒、消去時間は１０ミリ秒であり、前記実施の形態１と同様の十分に安定したリテンション特性を確認することができた。

【０１３０】以上、本発明者によってなされた発明を前記実施の形態に基づき具体的に説明したが、本発明は前記実施の形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。

【０１３１】本発明の不揮発性メモリは、セル構造が単純で、製造プロセスも簡略であることから、同一半導体基板上に不揮発性メモリとロジックＬＳＩとを混載するＬＳＩへの適用も容易である。

【０１３２】

【発明の効果】本願によって開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば、以下の通りである。

【０１３３】本発明の不揮発性メモリは、メモリセルが単一のＭＩＳＦＥＴで構成されているために、書き込み／消去動作を比較的簡便に行うことができ、必要とする周辺回路の面積を増加させることがない。また、製造工程も簡略である。

【０１３４】本発明の不揮発性メモリは、書き込み動作の際、ゲート電極とドレインとに正電圧を印加し、ソース近傍で発生させたホットエレクトロンを窒化シリコン膜中の電子トラップに注入する方式を採用するため、接地電位のソースとゲート電極間の電位差が大きくなることによって注入効率が向上し、従来のセル構造に比べてより低電圧での動作が可能となる。

【０１３５】本発明の不揮発性メモリの製造方法は、メモリセルのソース側のゲート絶縁膜（酸化シリコン膜、窒化シリコン膜、酸化シリコン膜からなる３層の絶縁膜）をゲート電極に対して自己整合（セルフアライン）で形成するので、従来のフローティングゲート型メモリセルと同等のセル面積に設計することができ、スケーラビリティに優れた不揮発性メモリを実現することができる。

【図面の簡単な説明】

【図１】本発明の実施の形態１であるフラッシュメモリの主要部を示す概略回路図である。

【図２】本発明の実施の形態１であるフラッシュメモリの要部を示す断面図である。

【図３Ａ】本発明の実施の形態１であるフラッシュメモリの導体層パターンを示す平面図である。

【図３Ｂ】本発明の実施の形態１であるフラッシュメモリの導体層パターンを示す平面図である。

【図４】本発明の実施の形態１であるフラッシュメモリのプログラム動作を説明する概略断面図である。

【図５】本発明の実施の形態１であるフラッシュメモリのプログラム動作を説明する動作電圧表である。

【図６】本発明の実施の形態１であるフラッシュメモリの書き込み動作時におけるチャネル領域の電位分布と電界強度分布とを示すグラフである。

【図７】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。

【図８】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。

【図９】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。

【図１０】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。
【図１１】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。
【図１２】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。
【図１３】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。
【図１４】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。
【図１５】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。
【図１６】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。
【図１７】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。
【図１８】本発明の実施の形態１であるフラッシュメモリの製造方法を示す要部断面図である。
【図１９】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図２０】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図２１】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図２２】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図２３】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図２４】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図２５】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図２６】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図２７】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図２８】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図２９】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図３０】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図３１】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図３２】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図３３】本発明の実施の形態２であるフラッシュメモリの製造方法を示す要部断面図である。
【図３４】本発明の実施の形態２であるフラッシュメモリの製造方法を示すフロー図である。

【図３５】本発明の実施の形態３であるフラッシュメモリの概略断面図である。
【図３６】本発明の実施の形態４であるフラッシュメモリの概略断面図である。
【図３７】本発明の実施の形態５であるフラッシュメモリの概略断面図である。
【図３８】本発明の実施の形態５であるフラッシュメモリのプログラム動作を説明する動作電圧表である。
【図３９】本発明の実施の形態６であるフラッシュメモリの概略断面図である。
【図４０】本発明の実施の形態６であるフラッシュメモリのプログラム動作を説明する動作電圧表である。
【図４１】本発明の実施の形態６であるフラッシュメモリの書き込み動作時における電圧印加の時間変化を示すグラフである。
【図４２】本発明の実施の形態６であるフラッシュメモリの書き込み動作時におけるチャネル領域の電位分布と電界強度分布とを示すグラフである。
【図４３】本発明の実施の形態７であるフラッシュメモリの概略断面図である。
【図４４】本発明の実施の形態８であるフラッシュメモリのセル構造を示す要部平面図である。
【図４５】図４４のＡ－Ａ’線に沿った半導体基板の要部断面図である。
【図４６】本発明の実施の形態８であるフラッシュメモリの製造方法を示す要部断面図である。
【図４７】本発明の実施の形態８であるフラッシュメモリの製造方法を示す要部断面図である。
【図４８】本発明の実施の形態８であるフラッシュメモリの製造方法を示す要部断面図である。
【図４９】本発明の実施の形態８であるフラッシュメモリの製造方法を示す要部断面図である。
【図５０】本発明の実施の形態８であるフラッシュメモリの製造方法を示す要部断面図である。
【図５１】本発明の実施の形態８であるフラッシュメモリの製造方法を示す要部断面図である。
【図５２】フローティングゲート型メモリセルのセル構造を示す概略断面図である。
【図５３】ＭＮＯＳ型メモリセルのセル構造を示す概略断面図である。
【図５４】選択用ゲート電極とサイドウォールゲート電極とを有するメモリセルのセル構造を示す概略断面図である。
【図５５】図５４に示すフラッシュメモリの書き込み動作時におけるチャネル領域の電位分布と電界強度分布とを示すグラフである。
【符号の説明】
１　半導体基板
２　フィールド酸化膜
３　酸化シリコン膜

4　(深い) n型ウエル
5　p型ウエル
6　n型ウエル
7　酸化シリコン膜
8　窒化シリコン膜
9　酸化シリコン膜
10a、10b、10c　ゲート電極
11　n^- 型半導体領域
12　p^- 型半導体領域
13　n^+ 型半導体領域
14　p^+ 型半導体領域
15　n^+ 型半導体領域
16　サイドウォールスペーサ
17　酸化シリコン膜
20～22コンタクトホール
23～27　配線
30　ゲート酸化膜
31a、31b、31c　ゲート電極
32　窒化シリコン膜
33　酸化シリコン膜
34　酸化シリコン膜
35　酸化シリコン膜
36　窒化シリコン膜
37　n^- 型半導体領域
38　p^- 型半導体領域
39　n^+ 型半導体領域
40　p^+ 型半導体領域
41　n^+ 型半導体領域
42　サイドウォールスペーサ
43　シリサイド層
44　酸化シリコン膜
45～47コンタクトホール
48～52　配線60　酸化シリコン膜
70　下部ゲート酸化膜
71　窒化シリコン膜
72　上部ゲート酸化膜
73　ゲート電極
74　n^- 型半導体領域
75　n^+ 型半導体領域
76　n^+ 型半導体領域
77　ゲート酸化膜
78　ゲート電極
79　n^+ 型半導体領域
80　下部ゲート酸化膜
81　窒化シリコン膜
82　(上部) ゲート酸化膜
83　ゲート電極
84　n^+ 型半導体領域
85　p^- 型半導体領域
86　n^+ 型半導体領域

87　n^- 型半導体領域
90　ゲート電極
91　p^- 型半導体領域
92　n^+ 型半導体領域 (ソース、ドレイン)
93　窒化シリコン膜 (キャップ)
94　サイドウォールスペーサ
95　酸化シリコン膜
96、97　コンタクトホール
98　プラグ
99　酸化シリコン膜
101　シリコン基板
102　ゲート酸化膜
103　フローティングゲート
104　層間絶縁膜
105　コントロールゲート
106　ソース
107　ドレイン
108　電子
111　シリコン基板
112　直接トンネル酸化膜
113　窒化シリコン膜
114　ゲート酸化膜
115a、115b　ゲート電極
116　ソース
117　接続拡散層ドレイン
118　ゲート酸化膜
119　ドレイン
121　シリコン基板
122　ゲート酸化膜
123　選択用ゲート電極
124　酸化シリコン膜
125　窒化シリコン膜
126　酸化シリコン膜
127　サイドウォールゲート電極
128　ソース
129　ドレイン
CSL　共通ソース線
DL (DL1 ～DLn)　ビット線
MA　メモリセルアレイ
M (M11～Mnm)　メモリセル
Qc　MISFET
Qm　MISFET
Qs　選択用MISFET
SL (SL1 ～SLm/2)　ソース線
SA　センスアンプ
WL (WL1 ～WLm)　ワード線
X－DEC　ロウデコーダ
Y－DEC　カラムデコーダ

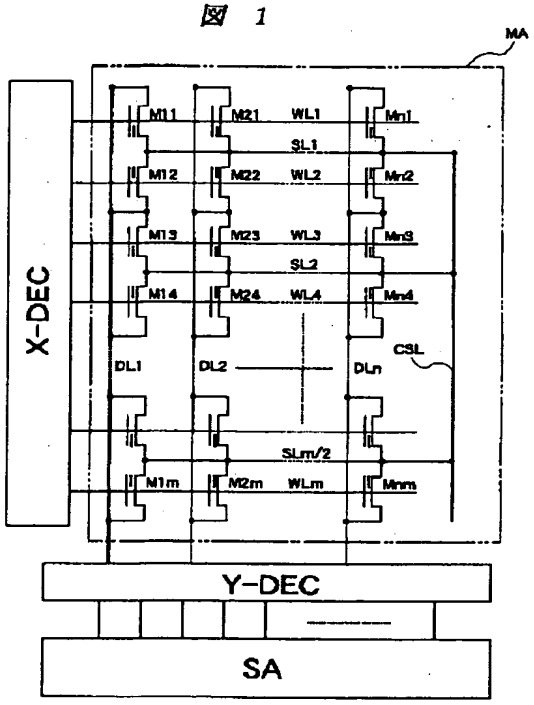
【要約】
【課題】　フローティングゲート型メモリセルに匹敵す

るスケーラビリティと、MNOS型メモリセルと同等以上の高い信頼性とを併せ持った新規なセル構造の不揮発性メモリおよびその製造方法を提供する。

【解決手段】　不揮発性メモリを構成するMISFET Qmは、ゲート絶縁膜上に形成されたゲート電極10aと、一端がゲート電極10aの下部まで延在するn$^+$型半導体領域13（ドレイン）と、ゲート電極10aに対してオフセットするように形成されたn$^+$型半導体領域15（高濃度ソース）と、一端がゲート電極10aの下部まで延在するn$^-$型半導体領域11（低濃度ソース）とで構成される。ゲート絶縁膜は、ドレイン側が1層の酸化シリコン膜9で構成され、ソース側が酸化シリコン膜7と窒化シリコン膜8と酸化シリコン膜9とを積層した3層の絶縁膜で構成される。

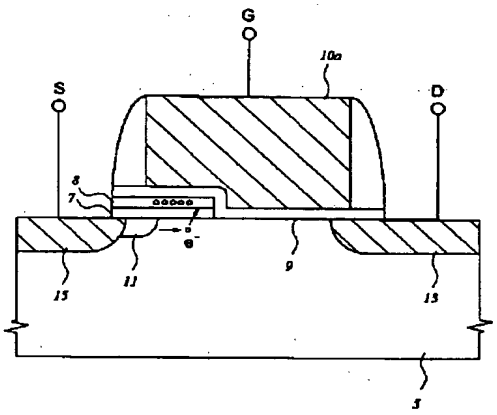
【図1】

図 1



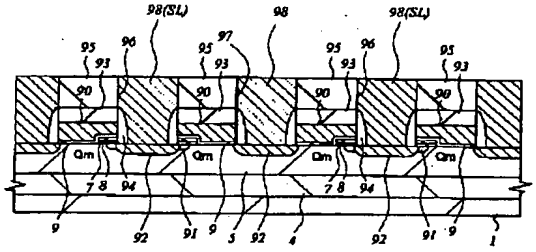
【図4】

図 4



【図51】

図 51



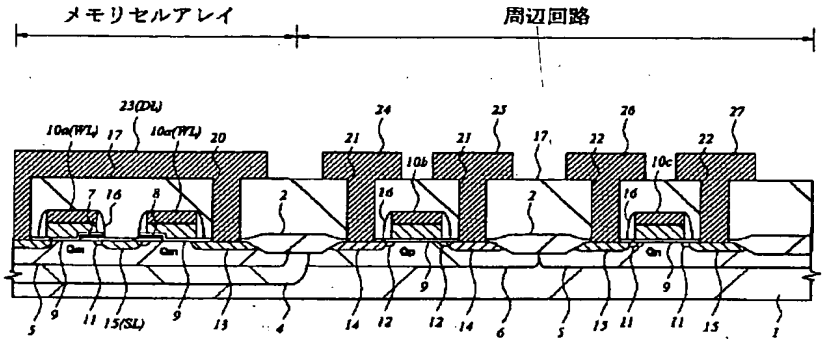
【図5】

図 5

端子	ビット線（ドレイン電圧）		ワード線（ゲート電圧）		ソース線	ウエル
	選択	非選択	選択	非選択		
書込み	5V	0V	5V	0V	0V	0V
消去	0V	0V	-10V	0V	5V	5V
読み出し	2V	0V	2V	0V	0V	0V

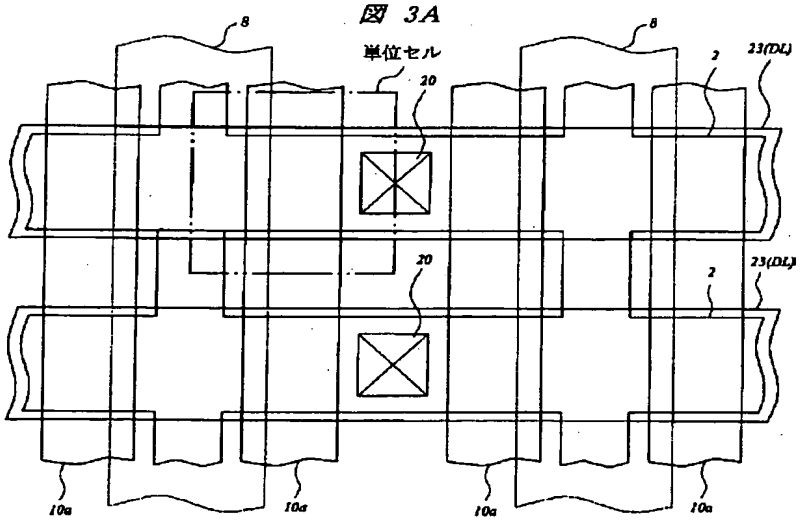
【図２】

図 2


メモリセルアレイ
周辺回路
23(DL)
10a(WL)
17
10a(WL)
20
24
21
25
21
17
26
22
27
10b
10c
22
7
16
8
16
16
2
2
Qm
Qm
Qp
Qn
9
9
9
5
9
11
15(SL)
9
13
4
14
12
12
14
6
5
13
11
11
15
1

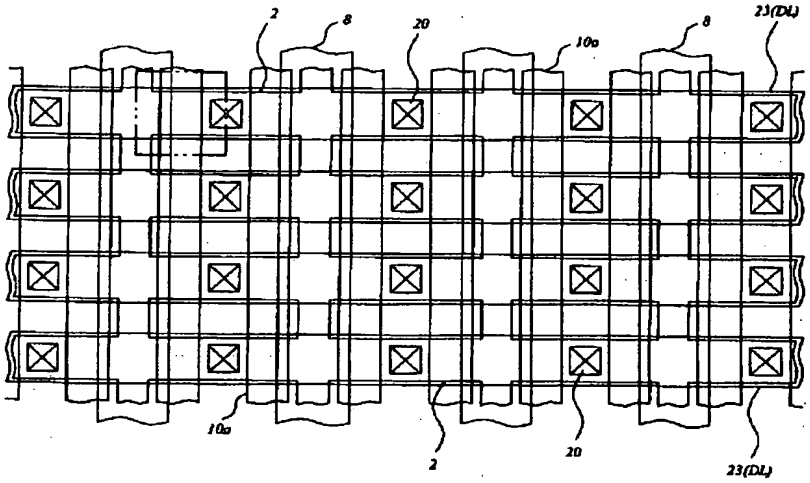
【図３Ａ】

図 3A


8
単位セル
20
8
2
23(DL)
20
2
23(DL)
10a
10a
10a
10a

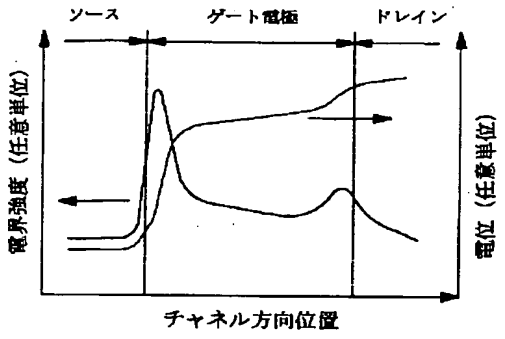
【図３Ｂ】

図 3B


2
8
20
10a
8
23(DL)
10a
2
20
23(DL)

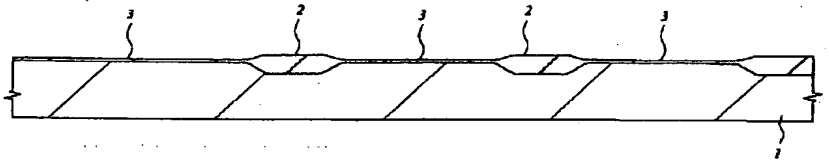
【図６】

図 6


ソース
ゲート電極
ドレイン
電界強度（任意単位）
電位（任意単位）
チャネル方向位置

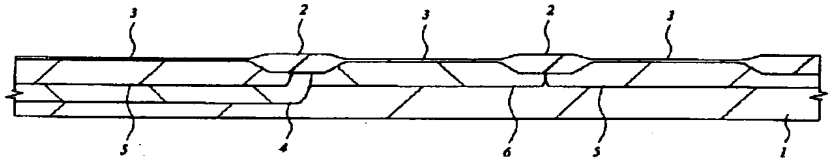
【図7】

図 7



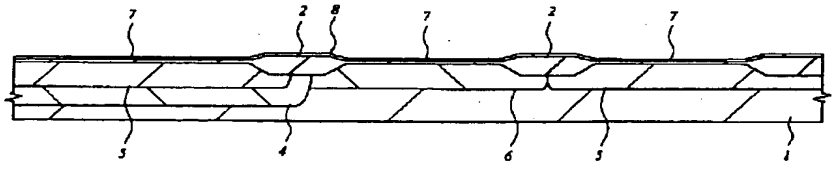
【図8】

図 8



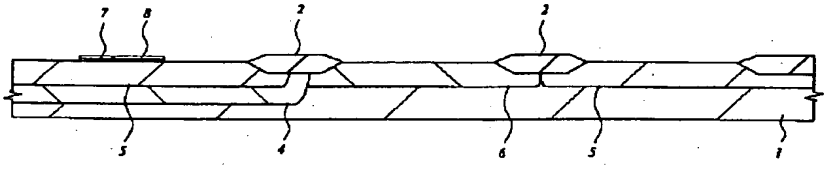
【図9】

図 9



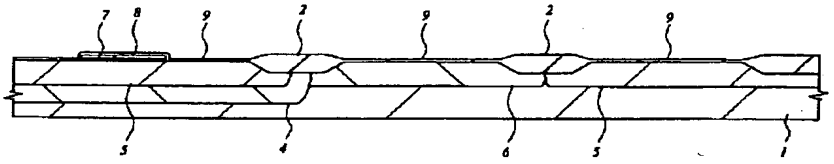
【図１０】

図 10



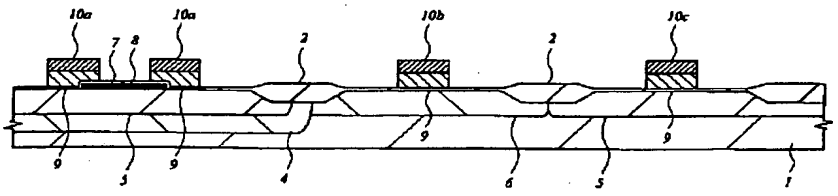
【図１１】

図 11



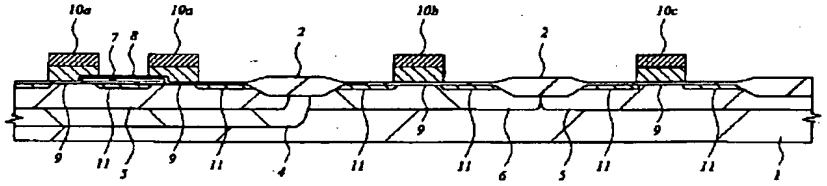
【図１２】

図 12



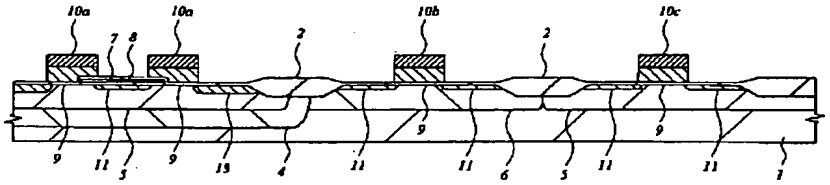
【図１３】

図 13



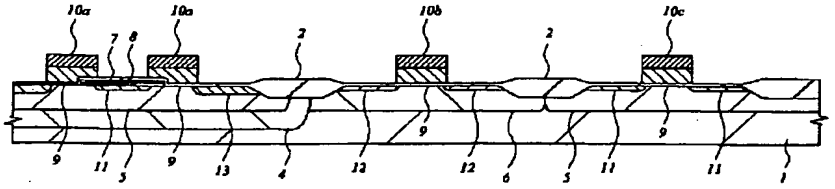
【図１４】

図 14



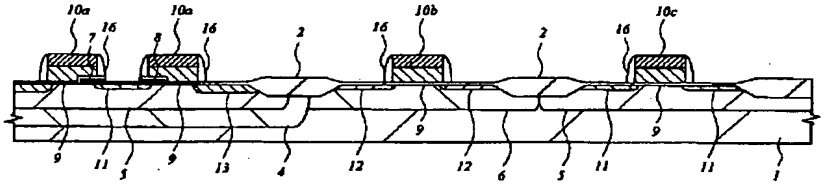
【図１５】

図 15



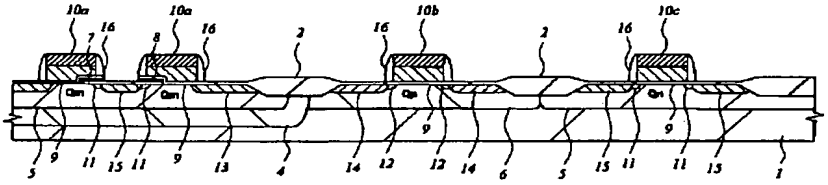
【図１６】

図 16



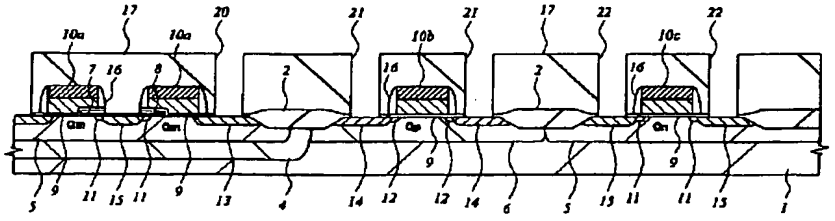
【図１７】

図 17



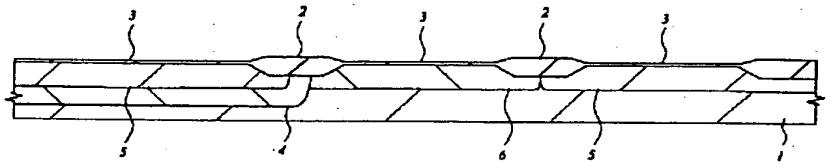
【図１８】

図 18



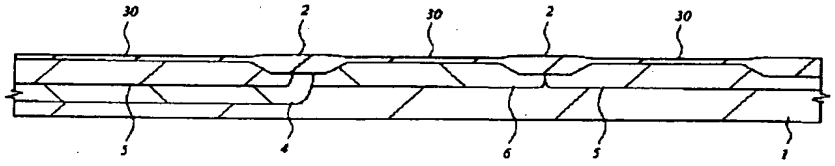
【図１９】

図 19



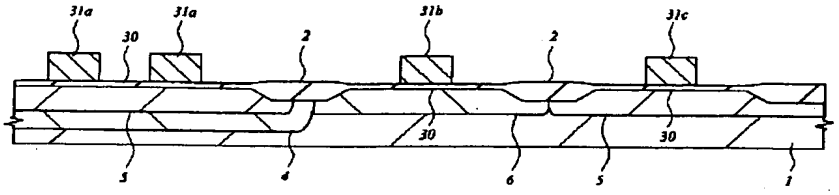
【図２０】

図 20



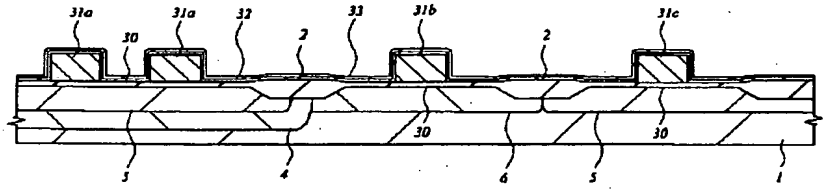
【図２１】

図 21



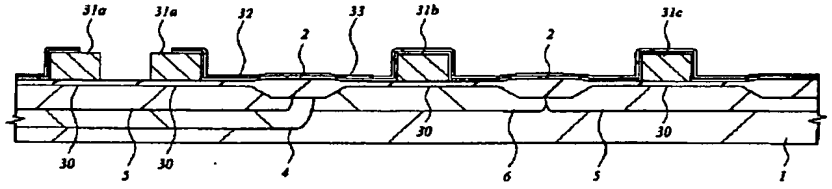
【図２２】

図 22



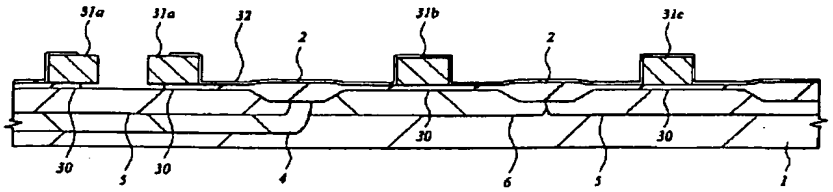
【図２３】

図 23



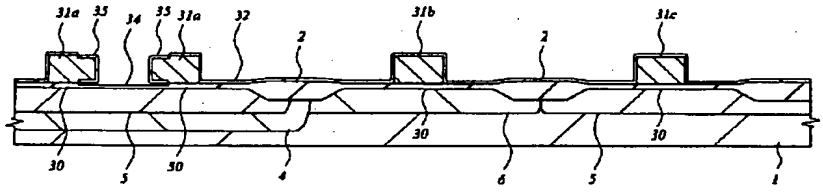
【図２４】

図 24



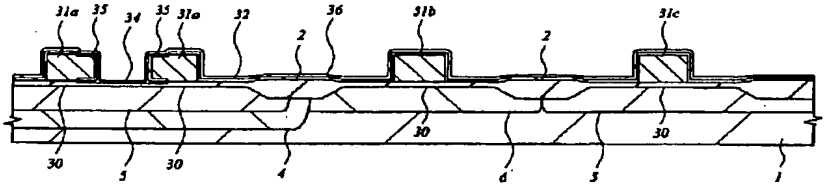
【図２５】

図 25



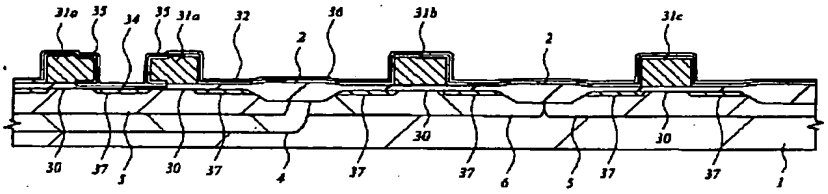
【図２６】

図 26



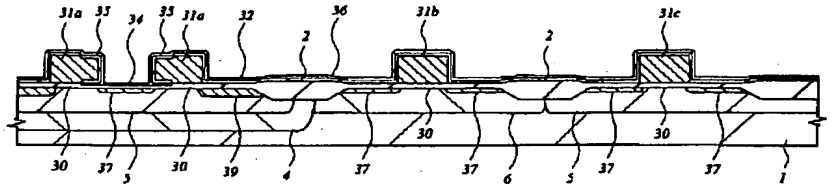
【図２７】

図 27



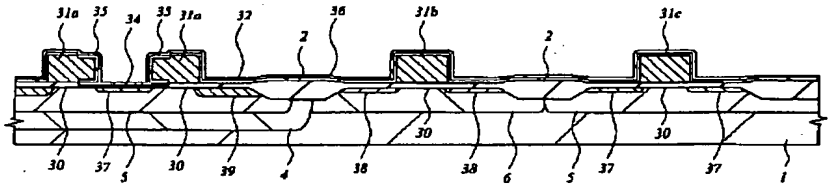
【図２８】

図 28



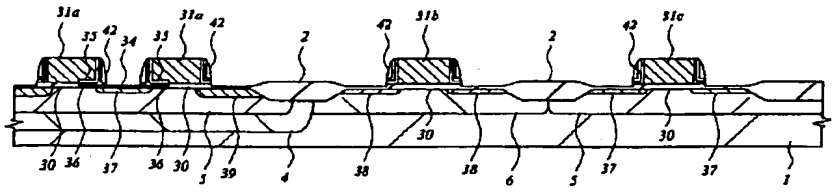
【図２９】

図 29



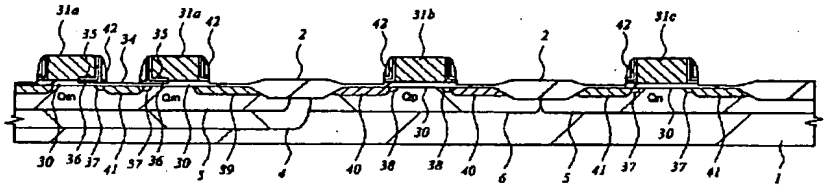
【図３０】

図 30



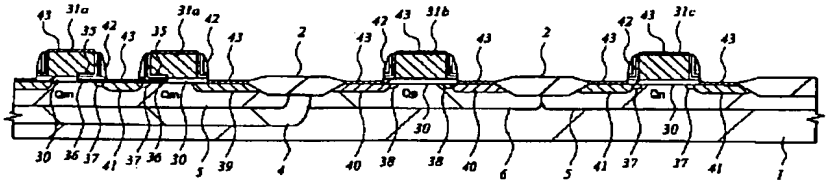
【図３１】

図 31



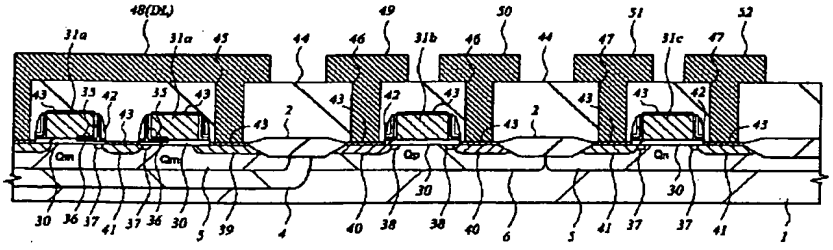
【図３２】

図 32



【図３３】

図 33



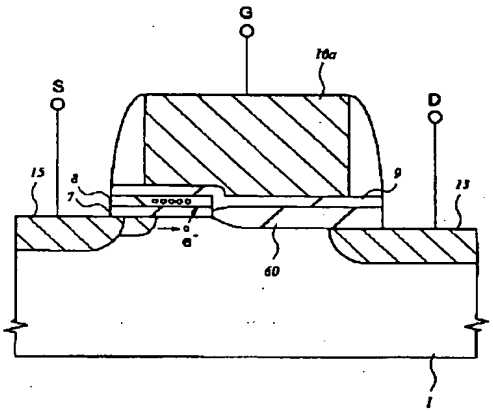
【図３４】

図 34

1. アイソレーション形成
2. 深いｎ型ウエルインプラ
3. 浅いｎ型ウエルインプラ
4. ｐ型ウエルインプラ
5. ゲート電極加工
6. [illegible]
7. [illegible]
8. 周辺ｐＭＯＳ低濃度ソース、ドレインインプラ
9. ｎ+型半導体領域インプラ
10. ｐ+型半導体領域インプラ
11. コンタクトホール開孔
12. 第１メタル配線加工

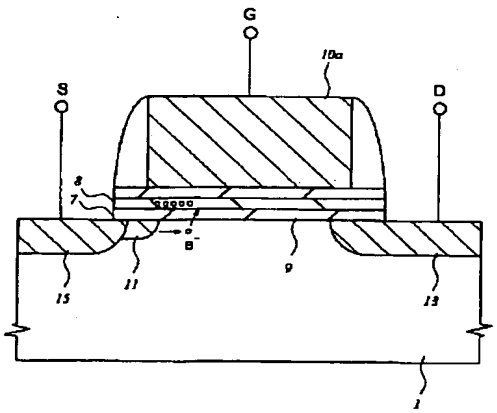
【図３５】

図 35



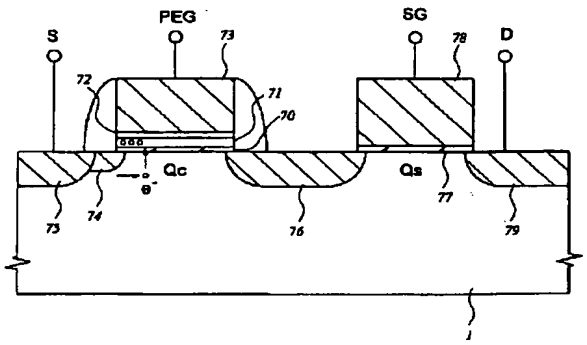
【図３６】

図 36



【図３７】

図 37



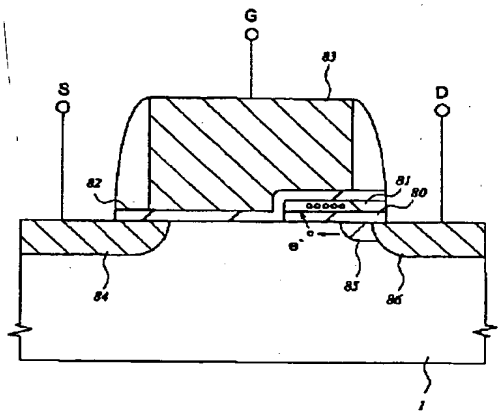
【図３８】

図 38

端子	ビット線 (D)		ワード線 (SG)		書込消去線 (PEG)		ソース線 (S)	ウエル
	選択	非選択	選択	非選択	選択	非選択		
書込み	5V	0V	2V	0V	5V	0V	0V	0V
消去	0V	0V	0V	0V	-10V	0V	5V	5V
読み出し	2V	0V	2V	0V	2V	0V	0V	0V

【図３９】

図 39



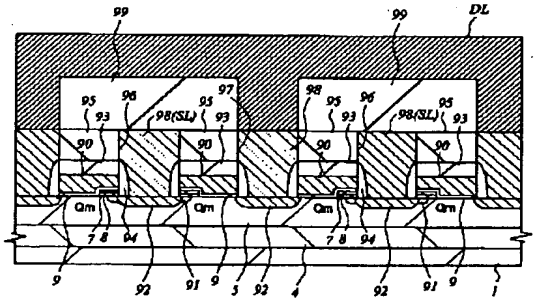
【図４０】

図 40

端子	ビット線 (ドレイン電圧)		ワード線 (ゲート電圧)		ソース線	ウエル
	選択	非選択	選択	非選択		
書込み	0V	5V	5V	0V	5V	0V
消去	0V	0V	-10V	0V	5V	5V
読み出し	2V	0V	2V	0V	0V	0V

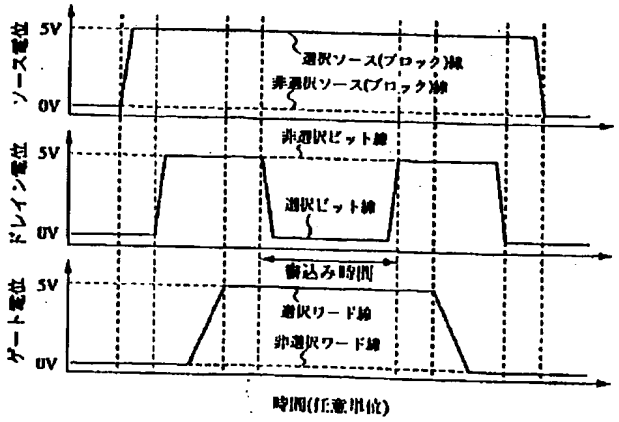
【図４５】

図 45



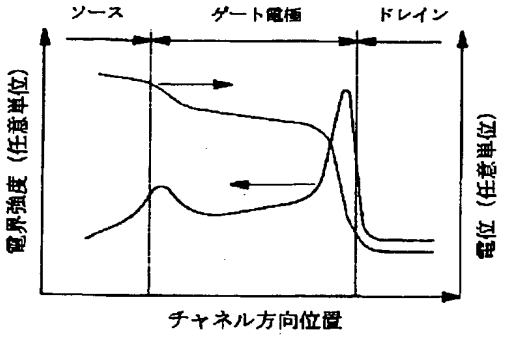
【図４１】

図 41



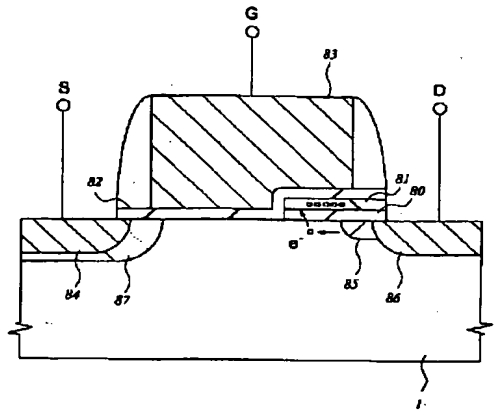
【図４２】

図 42



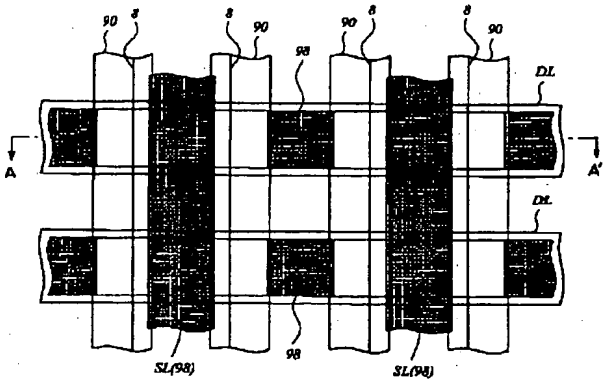
【図４３】

図 43



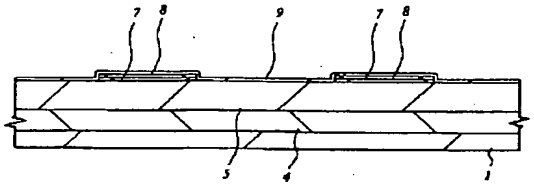
【図４４】

図 44



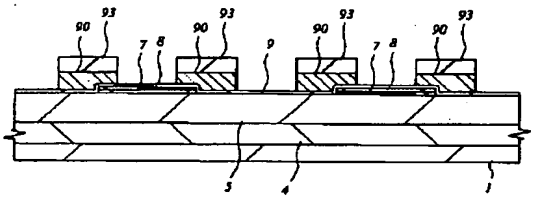
【図４６】

図 46



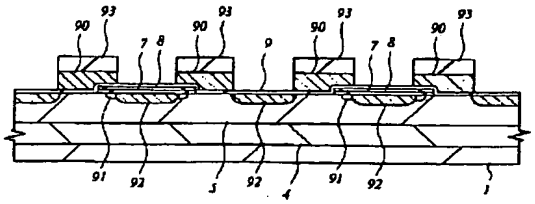
【図４７】

図 47



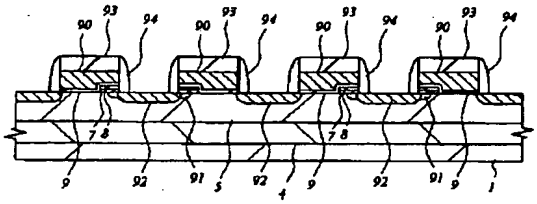
【図４８】

図 48



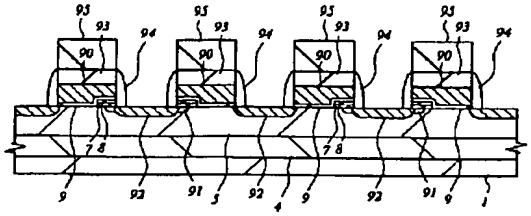
【図４９】

図 49



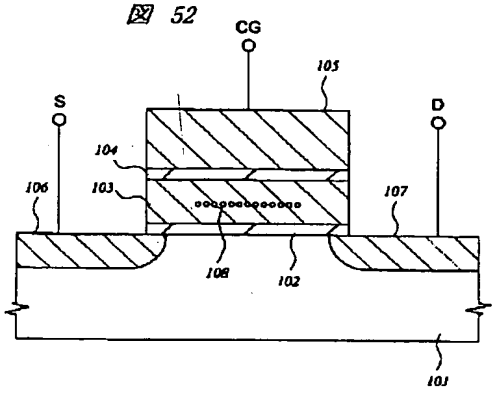
【図５０】

図 50



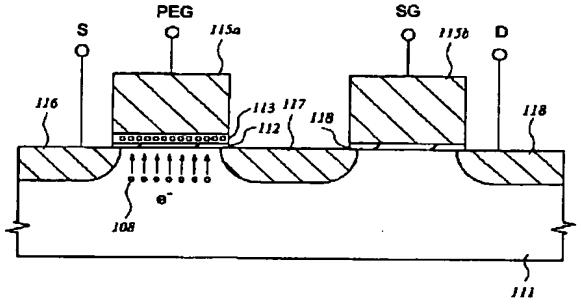
【図５２】

図 52



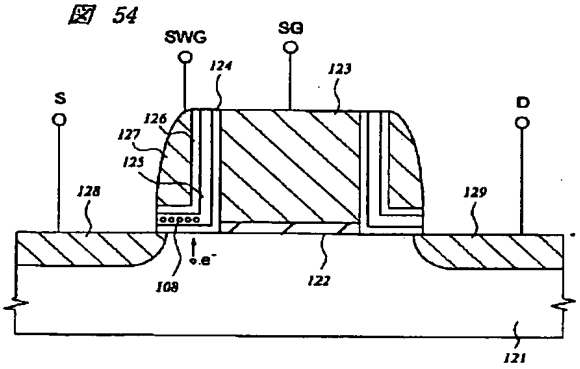
【図５３】

図 53



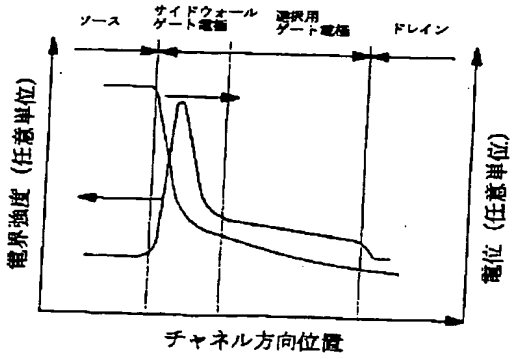
【図５４】

図 54



【図５５】

図 55



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(58)調査した分野(Int.Cl.^{6}，ＤＢ名)
H01L 27/115
H01L 21/8247
H01L 29/788
H01L 29/792

(19) Japan Patent Office (JP)

(11) Patent Number

(12) Public Patent Announcement (B1) No. 2978477

(45) Date Issued: November 15, 1999

(24) Date Registered: September 10, 1999

(51) Int. Cl.[6]	ID Code	FI		
H 01 L 27/115		H 01 L	27/10	434
21/8247			29/78	371
29/788				
29/792				

Number of claims: 19 (Altogether 33 pages)

(21) Application No.: Pat App Hei 10-165733

(22) Application Date: June 12, 1998

Examination Request Date: June 12, 1998

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Examiner: Asahi Shozan

Continued to the final page.

(54) [Title of the Invention] A semiconductor integrated circuit device and its manufacturing method

(57) [Scope of the Patent Claims]

[Claim 1]

A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs, and where a gate electrodes connected electrically to word lines are formed on a gate insulation film, formed on a first conductive type semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising source and drain regions, are formed in the

semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. The semiconductor integrated circuit device is characterized by the fact that the gate insulation film consists, at least in the first semiconductor region side, of three layers of insulation films where a silicon oxide film, a silicon nitride film, and the second silicon oxide film are accumulated, and that writing into the memory cell is performed by setting the second semiconductor region at a higher potential than the first semiconductor region.

[Claim 2]

A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs, and where the gate electrodes connected electrically to word lines are formed on a gate insulation film formed on a semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising a source and a drain region are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. A semiconductor integrated circuit device characterized by the fact that the gate insulation film consists, at least in the first semiconductor region side, of three layers of insulation films where a silicon oxide film, a silicon nitride film, and a second silicon oxide film are accumulated, also that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is lower than the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region, and that hot electrons are injected to the silicon nitride film by generating the hot electrons in the first semiconductor region side.

[Claim 3]

A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs, and where the gate electrodes connected electrically to word lines are formed on a gate insulation film formed on a semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising a source and drain regions are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. A semiconductor integrated circuit device characterized by the fact that the gate insulation film consists, in the first semiconductor region side, of three layers of insulation films where a silicon oxide film, a silicon nitride film, and a second silicon oxide film are accumulated. The second semiconductor region side consists of a silicon oxide film, and that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is different from the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region.

[Claim 4]

A semiconductor integrated circuit device described in Claim 1 or 3, characterized by the fact that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is lower than the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region.

[Claim 5]

A semiconductor integrated circuit device described in Claim 1, 2, or 4, characterized by the fact that the gate insulation film is made of three layers of insulation films comprising a first silicon oxide film, a silicon nitride film, and a second silicon oxide film are accumulated in the first semiconductor region side, and a silicon oxide film in the second semiconductor region side.

[Claim 6]

A semiconductor integrated circuit device described in one of the Claims 1~5, where a semiconductor integrated circuit device is characterized by the fact that the gate insulation film has the first semiconductor region side and the second semiconductor region side having almost the same electric capacity film thickness.

[Claim 7]

A semiconductor integrated circuit device described in Claim 1, 2, 4, 5, or 6, where a semiconductor integrated circuit device is characterized by the fact that the gate insulation film has the first semiconductor region side and the second semiconductor region side consisting of three layers of insulation films consisting of a first silicon oxide film, a silicon nitride film, and a second silicon oxide film are accumulated.

[Claim 8]

A semiconductor integrated circuit described in Claim 1, 3, 4, 5, 6, or 7, where a semiconductor integrated circuit device is characterized by the fact that writing into the memory cell is performed by injecting hot electrons into the silicon nitride film composing a part of the gate insulation film.

[Claim 9]

A semiconductor integrated circuit device described in one of the Claims 1~8, where a semiconductor integrated circuit device is characterized by the fact that among the three layers of insulation film composing at least a part of the gate insulation film, the film thickness of the first silicon oxide film formed in the lower layer of the silicon nitride film is thicker than the film thickness that direct tunnel current flows.

[Claim 10]

A semiconductor integrated circuit device described in one of the Claims 1~9, where a semiconductor integrated circuit device is characterized by the fact that the second semiconductor region consists of a first conductive type semiconductor region whose one end extends to the lower part of the gate electrodes and a second conductive type semiconductor region whose one end is separated from the gate electrodes, where the first semiconductor region is made of the second conductive type.

[Claim 11]

A semiconductor integrated circuit device described in one of the Claims 1~10, where a semiconductor integrated circuit device is characterized by the fact that reading out of the memory cell is performed by setting the first semiconductor region at higher potential than the second semiconductor region.

[Claim 12]

A semiconductor integrated circuit device described in one of the Claims 1~10, where a semiconductor integrated circuit device is characterized by the fact that reading out of the memory

cell is performed by setting the second semiconductor region at higher potential than the first semiconductor region.

[Claim 13]

A semiconductor integrated circuit device described in one of the Claims 1~12, where a semiconductor integrated circuit device is characterized by the fact that a source line is formed by a plug embedded in the first connection hole formed on the upper insulation film in one of the first and second semiconductor regions, and that bit lines are connected to the other of the first and second semiconductor regions via a plug embedded in the second connection hole formed on the insulation film in the upper part of the other of the first and second semiconductor regions.

[Claim 14]

A semiconductor integrated circuit device described in Claim 13, where a semiconductor integrated circuit device is characterized by the fact that the first connection hole and the second connection hole are formed self-aligned to the space of the gate electrodes of the MISFET.

[Claim 15]

A semiconductor integrated circuit device described in one of the Claims 1~14, where a semiconductor integrated circuit device is characterized by the fact that the memory cell consists of the MISFET comprising a memory element section and a selection MISFET.

[Claim 16]

A semiconductor integrated circuit device described in one of the Claims 1~9 and 11~15, where a semiconductor integrated circuit device is characterized by the fact that the first semiconductor region and the second semiconductor region are the same conductive type.

[Claim 17]

A semiconductor integrated circuit device manufacturing method characterized by the following processes:
(a) a process where, after forming the second silicon oxide film on a semiconductor substrate, the gate electrodes of MISFET are formed by patterning a conductor film formed on the top of the second silicon oxide film,
(b) a process where, after forming the second silicon nitride film on the semiconductor substrate containing the upper part of the gate electrodes, the fourth silicon oxide film is formed on the top of the second silicon nitride film,
(c) a process of exposing the upper part and side walls of the gate electrodes of the MISFET by etching the fourth silicon oxide film and the second silicon nitride film,
(d) a process of exposing the bottom face of the gate electrodes and the semiconductor substrate in the first region of the lower part of the gate electrodes and leaving the second silicon oxide film in the second region of the lower part of the gate electrodes by isotropically etching the second silicon oxide film,
(e) a process of forming the first silicon oxide film on the top face of the semiconductor substrate and the bottom face of the gate electrodes in the first region by thermally processing the semiconductor substrate, and

(f) a process of forming the second silicon nitride film on the semiconductor substrate containing a space between the first silicon oxide film formed on the top face of the semiconductor substrate and the first silicon oxide film formed on the bottom face of the gate electrodes in the first region.

[Claim 18]

Being a semiconductor integrated circuit device manufacturing method described in Claim 17, a semiconductor integrated circuit device manufacturing method characterized by the fact that it contains a process of introducing an self-aligned impurity to the end of the first region side of the gate electrodes to form the first semiconductor region in the semiconductor substrate and a process of introducing an self-aligned impurity to the end of the second region side of the gate electrodes to form the second semiconductor region in the semiconductor substrate, and that the impurity concentration in the first semiconductor region is set lower than the impurity concentration in the second semiconductor region.

[Claim 19]

Being a semiconductor integrated circuit device manufacturing method described in Claim 17 or 18, a semiconductor integrated circuit device manufacturing method characterized by the fact that the MISFET comprises a nonvolatile memory, that the gate electrodes of the MISFET comprising a peripheral circuit and the gate electrodes of the MISFET comprising the nonvolatile memory are formed in a process of patterning the same conductive film, and that the gate electrodes of the MISFET comprising the peripheral circuit are formed in a process of forming the second silicon oxide film.

[Detailed Explanation of the Invention]
[0001]
[Field of Technology]

This invention relates to a semiconductor integrated circuit device and its manufacturing technology, especially a technology effectively applicable to semiconductor integrated circuit devices which have a nonvolatile memory of the single MISFET structure that makes the insulation film trap a charge accumulation region.

[0002]
[Prior Art]

The basic cell structure of a nonvolatile memory formed on a silicon substrate is classified into two large categories: the floating gate type where a floating gate is installed between a gate oxide film and a control gate (word lines) above it and being electrically isolated from the surroundings is made a charge accumulation region, and an MNOS (Metal-gate Nitride Oxide Silicon) type where having no such floating gate, a gate insulation film is made of a cumulate film of a silicon oxide film and a silicon nitride film, and the electrons trapped in the silicon nitride film are made a charge accumulation region.

[0003]

Figure 52 is a cross-sectional view showing a representative cell structure of a floating gate type memory. This memory cell has a structure where a floating gate 103, an interlayer insulation film 104, and a control gate (CG) 105 are formed sequentially on the top of a gate oxide film 102 with a

film thickness of about 10 nm formed on the main surface of a silicon substrate 101, and a source (S) 106 and a drain (D) 107 are formed on the silicon substrate 101 on both sides of the floating gate 103.

[0004]

Writing into each memory cell is performed by injecting electrons 108 into the floating gate 103 and increasing the threshold voltage (Vth) of the transistor seen from the control gate 105 by 3V~5V compared with the condition where there is no accumulation of electrons 108. Also, the mainstream method of injecting electrons 108 into the floating gate 103 is to draw hot electrons generated by the avalanche breakdown near the drain 107 into the floating gate 103 by a positive voltage charged to the control gate 105.

[0005]

On the other hand, Fig. 53 is a cross-sectional view showing a representative cell structure of a MNOS-type memory cell. This memory cell consists of a MISFET (memory element section) where a silicon nitride film 113 and a writing/erasing gate electrode (PEG) 115a are formed sequentially on the top of a direct tunnel oxide film 112 with a film thickness of about 2 nm formed on the main surface of a silicon substrate 111 and a source (S) 116 and a connecting diffusion layer (drain) 117 are formed on the silicon substrate 111 on both sides of the gate electrode 115a. A selection MISFET where a selection gate electrode (SG) 115b on the top of the gate oxide film 118 is formed and a connecting diffusion layer (source) 117 and a drain (D) 119 are formed on the silicon substrate 111 on both sides of the gate electrode 115b.

[0006]

Writing into each memory cell is performed by increasing the threshold voltage of the MISFET in the memory element section through controlling the potential of the silicon substrate 111 and the writing/erasing gate electrode 115a to inject electrons 108 from the silicon substrate 111 side via the direct tunnel oxide film 112 onto the whole surface of the silicon nitride film 113 and make them trapped. Also, erasing is performed in the same way by decreasing the threshold voltage of the MISFET in the memory element section through controlling the potential of the silicon substrate 111 and the writing/erasing gate electrode 115a to eject electrons trapped in the silicon nitride film 113 to the silicon substrate 111 side. In this erasing operation, because the threshold voltage of the memory element section is lowered to below 0 V, namely down to the depression region, the selection MISFET becomes necessary other than the MISFET in the memory element section for reading out.

[0007]

Because the NMOS-type memory cell has an operation scheme of trapping electrons inside an insulation film (silicon nitride film 113), trapped electrons contribute to the modulation of the threshold voltage independently. Therefore, a variation of the threshold voltage over the entire channel region of the memory element section due to partial leakage of electrons inside the silicon nitride film 113 caused by defects inside the tunnel film 112 is very small. In other words, its retention property is excellent, and it can be to be a highly reliable memory cell scheme.

[0008]

Figure 54 is a cross-sectional view showing a cell structure named "Self-Aligned Split-Gate EEPROM Device" described in USP No. 5408115. This memory cell has a structure where a gate oxide film

122 and a selection gate electrode (SG) 123 are accumulated on the main surface of a silicon substrate 121. A side wall gate electrode (SWG) 127 is formed on those side walls via a three-layer insulation film consisting of a silicon oxide film 124, silicon nitride film 125, and a silicon oxide film 126. Also, a source (S) 128 is formed by ion injection masked with this side wall gate electrode (SWG) 127, and a drain (D) 129 is formed by ion injection masked with the selection gate electrode 123.

[0009]

As described in "1997 Symposium on VLSI Technology Digest of Technical Papers p63-p64", writing into a memory cell is performed by charging the source 128, side wall gate electrode 127, and selection gate electrode 123 with voltages of 5 V, 9 V, and 1 V, respectively with the drain 129 as the ground level.

[0010]

Figure 55 shows the potential distribution and electric field intensity distribution of the channel region in the writing operation of the memory cell. Because the voltage (5 V) charged between the source (S) and drain (D) is mostly charged to a void layer of the source, the electric field intensity along the channel direction becomes maximum immediately below the side wall gate electrode (SWG) as shown in the figure. Therefore, electrons running from the drain (D) to the channel region are accelerated in a high electric field region near the source (S) leading to the avalanche breakdown, and hot electrons generated at this time are injected and trapped in the silicon nitride film (125) by a vertical high electric field caused by the side wall gate electrode (SWG). Namely, by electrons being trapped in the silicon nitride film (125) immediately below the side wall gate electrode (SWG), the threshold voltage seen from the side wall gate electrode (SWG) rises up. The writing scheme by these hot electrons is basically identical to the scheme where the hot electrons near the drain in the floating gate type memory cell are drawing into the floating gate.

[0011]

Also, in reading out of the memory cell, a voltage of 1.8 V is charged to the side wall gate electrode (127) and the selection gate electrode (123) with the source (128) as the ground level, and modulation of the threshold voltage seen from the side wall gate electrode (127) due to presence/absence of an electron trap in the silicon nitride film (125) is judged from the drain current. Because this memory cell performs writing using hot electrons, even if the silicon oxide film (124) immediately below the silicon nitride film that traps the electrons is formed with a thicker film thickness (about 10 nm for example) than the direct tunnel oxide film of the MNOS-type memory cell, the writing speed does not become degraded. Also, the thicker this silicon oxide film (124) is, the lower the defect density becomes, and the retention property of the memory cell improves as the result.

[0012]

IEEE Electron Device Lett., (vol. EDL-8, no. 3, pp. 93-95, March 1987) discloses a nonvolatile memory of the single MISFET structure which has no control gate. Memory cell of this nonvolatile memory consist of a gate electrode of polycrystalline silicon formed on the top of a gate insulation film, with a source and a drain formed on a semiconductor substrate on both sides of this gate electrode, and the gate insulation film consists of the three-layer structure where a silicon nitride film is sandwiched between two layers of silicon oxide film.

[0013]

Writing into each memory cell is performed by making the carriers near the drain to be injected into the silicon nitride film and trapped. This memory cell is excellent in its retention property compared with the MNOS-type memory cell because the carriers in the silicon nitride film sandwiched by two layers of silicon oxide films exist locally in a narrow region near the drain.

[0014]

Japanese Patent Disclosure Hei 6-232416 public report discloses nonvolatile memory of the single MISFET structure where a gate insulation film and a trap film that retains the carriers are formed in sequence on the top of a channel region between a source and a drain, and a gate electrode is formed on the top of this gate insulation film and trap film. The gate insulation film is made of a silicon oxide film, and the trap film consists of a three-layer structure where a silicon nitride film is sandwiched between two layers of silicon oxide film.

[0015]

Writing into each memory cell is performed by injecting electrons into a silicon nitride film and trapping them in a silicon oxide film (tunnel oxide film) of a bottom layer comprising a part of the trap film. Because this memory cell forms a gate insulation film of a normal enhancement MISFET and a trap film in the memory section that retains the carriers in the lower part of a single gate electrode, the cell area can be reduced.

[0016]

[Problems Overcome by the Invention]

The floating gate type memory cell described above can be designed with relatively a small cell area because a control gate (word lines) is accumulated on the top of a floating gate, having a cell structure fit for increasing the capacity. On the other hand, although the MNOS-type memory cell has an excellent retention property compared with the floating gate type memory cell, being regarded as a highly reliable cell scheme, because it requires two basic elements for a memory element section and selection, the cell area under the same design rule becomes 4~5 times larger than the floating gate type memory cell, having the shortcoming of not being fit for increasing the capacity.

[0017]

Also, the memory cell disclosed in USP No. 5408115 has comparable scalability to the floating gate type memory cell and a reliability equivalent to or higher than the MNOS-type memory cell. However, its cell structure having a selection gate electrode and a side wall gate electrode makes the writing/erasing operation complicated compared with the floating gate type memory cell, increasing the required peripheral circuit area as the result. Moreover, because the side wall gate electrode is about 100 nm in width, its wiring resistance increases to 5~7 times as large as normal gate resistance, introducing degradation of the read-out speed. Furthermore, although the channel region between the selection gate electrode and the side wall gate electrode, namely immediately below the region where a silicon oxide film (124), a silicon nitride film (125), and a silicon oxide film (126) are accumulated in the horizontal direction is as small as about 30 nm in width, and the gate electrode

does not exist on its top. Therefore, this region functions as a parasitic resistance, causing a problem of decreasing the drain current at read-out and degrading the read-out speed.

[0018]

The objective of this invention is to provide a nonvolatile memory equipped with a new cell structure having both scalability comparable to the floating gate type memory cell and the reliability equivalent or higher than the MNOS-type memory cell and its manufacturing method.

[0019]

This and other objectives and new characteristics of this invention will become evident from the descriptions in this specification and attached drawings.

[0020]

[Problem Resolution Means]

Among the inventions disclosed in this application, outlines of the representative ones are explained as follows.

[0021]

In the nonvolatile memory cell in this invention, is composed of MISFETs where gate electrodes connected electrically to word lines are formed on a gate insulation film, formed on a first conductive type semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising the source and drain regions are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. The gate insulation film consists, at least in the first semiconductor region side, of three layers of insulation films where the first silicon oxide film, a silicon nitride film, and the second silicon oxide film are accumulated.

[0022]

Writing into the memory cell is performed by setting the second semiconductor region at a higher electric level than the first semiconductor region in the selected memory cell and injecting hot electrons generated in the second conductive-type semiconductor region with a low impurity concentration into an electron trap in a silicon nitride film.

[0023]

Other than that, the inventions described in this application are explained item by item as follows.

[0024]

1. A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs, where the gate electrodes connected electrically to word lines are formed on a gate insulation film, formed on a first conductive type semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising the source and drain regions are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and

the second semiconductor region. A semiconductor integrated circuit device characterized by the fact that the gate insulation film consists, at least in the first semiconductor region side, of three layers of insulation films where a first silicon oxide film, a silicon nitride film, and the second silicon oxide film are accumulated, and that writing into the memory cell is performed by setting the second semiconductor region at a higher potential than the first semiconductor region.

[0025]

2. A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs where the gate electrodes connected electrically to word lines are formed on a gate insulation film, formed on a semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising the source and drain regions are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. A semiconductor integrated circuit device characterized by the fact that the gate insulation film consists, at least in the first semiconductor region side, of three layers of insulation films where a first silicon oxide film, a silicon nitride film, and the second silicon oxide film are accumulated, that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is lower than the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region, and that hot electrons are injected to the silicon nitride film by generating the hot electrons in the first semiconductor region side.

[0026]

3. A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs where the gate electrodes connected electrically to word lines are formed on a gate insulation film formed on a semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising the source and drain regions are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. A semiconductor integrated circuit device characterized by the fact that the gate insulation film consists, in the first semiconductor region side, of three layers of insulation films where the first silicon oxide film, a silicon nitride film, and the second silicon oxide film are accumulated, that the second semiconductor region side consists of a silicon oxide film, and that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is different from the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region.

[0027]

4. In Claim 1 or 3, a semiconductor integrated circuit device characterized by the fact that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is lower than the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region.

[0028]

5. In Claim 1, 2, or 4, a semiconductor integrated circuit device characterized by the fact that the gate insulation film is made of three layers of insulation films where the first silicon oxide film, silicon nitride film, and the second silicon oxide film are accumulated in the first semiconductor region side, and a silicon oxide film in the second semiconductor region side.

[0029]

6. In one of the Claims 1~5, a semiconductor integrated circuit device characterized by the fact that the gate insulation film has the first semiconductor region side and the second semiconductor region side having almost the same electric capacity film thickness.

[0030]

7. In Claim 1, 2, 4, 5, or 6, a semiconductor integrated circuit device characterized by the fact that the gate insulation film has the first semiconductor region side and the second semiconductor region side consisting of three layers of insulation films where the first silicon oxide film, silicon nitride film, and the second silicon oxide film are accumulated.

[0031]

8. In Claim 1, 3, 4, 5, 6, or 7, a semiconductor integrated circuit device characterized by the fact that writing into the memory cell is performed by injecting hot electrons into the silicon nitride film composing a part of the gate insulation film.

[0032]

9. In one of the Claims 1~8, a semiconductor integrated circuit device characterized by the fact that among the three layers of insulation film composing at least a part of the gate insulation film, the film thickness of the first silicon oxide film formed in the lower layer of the silicon nitride film is thicker than the film thickness that direct tunnel current flows.

[0033]

10. In one of the Claims 1~9, a semiconductor integrated circuit device characterized by the fact that the second semiconductor region consists of a first conductive type semiconductor region whose one end extends to the lower part of the gate electrodes and a second conductive type semiconductor region whose one end is separated from the gate electrodes, where the first semiconductor region is made of the second conductive type.

[0034]

11. In one of the Claims 1~10, a semiconductor integrated circuit device characterized by the fact that reading out of the memory cell is performed by setting the first semiconductor region at a higher potential than the second semiconductor region.

[0035]

12. In one of the Claims 1~10, a semiconductor integrated circuit device characterized by the fact that reading out of the memory cell is performed by setting the second semiconductor region at a higher potential than the first semiconductor region.

[0036]

13. In one of the Claims 1~12, a semiconductor integrated circuit device characterized by the fact that a source line is formed by a plug embedded in the first connection hole formed on the upper

insulation film in one of the first and second semiconductor regions, and that bit lines are connected to the other of the first and second semiconductor regions via a plug embedded in the second connection hole formed on the insulation film in the upper part of the other of the first and second semiconductor regions.

[0037]

14. In the Claim 13, a semiconductor integrated circuit device characterized by the fact that the first connection hole and the second connection hole are formed self-aligned to the space of the gate electrode of the MISFET.

[0038]

15. In one of the Claims 1~14, a semiconductor integrated circuit device characterized by the fact that the memory cell consists of the MISFET comprising a memory element section and a selection MISFET.

[0039]

16. In one of the Claims 1~9 and 11~15, a semiconductor integrated circuit device characterized by the fact that the first semiconductor region and the second semiconductor region are the same conductive type.

[0040]

17. A semiconductor integrated circuit device manufacturing method characterized by the following processes:
(a) a process where, after forming the first silicon oxide film on a semiconductor substrate, a silicon nitride film is formed on the first silicon oxide film, (b) a process where, by patterning the first silicon oxide film and the silicon nitride film, the first silicon oxide film and the silicon nitride film are left on the first region on the semiconductor substrate, and the first silicon oxide film and the silicon nitride film in the second region are removed, (c) a process of forming the second silicon oxide film on the top of the silicon nitride film in the first region on the semiconductor substrate and in the second region on the semiconductor substrate, and (d) a process where, by patterning a conductive film formed on the top of the second silicon oxide film, gate electrodes of MISFET is formed on the second silicon oxide film in the first and second regions.

[0041]

18. A semiconductor integrated circuit device manufacturing method characterized by the following processes:
(a) a process where, after forming the second silicon oxide film on a semiconductor substrate, the gate electrodes of MISFET are formed by patterning a conductor film formed on the top of the second silicon oxide film, (b) a process where, after forming the second silicon nitride film on the semiconductor substrate containing the upper part of the gate electrodes, the fourth silicon oxide film is formed on the top of the second silicon nitride film, (c) a process of exposing the upper part and side walls of the gate electrodes of the MISFET by etching the fourth silicon oxide film and the second silicon nitride film, (d) a process of exposing the bottom face of the gate electrodes and the semiconductor substrate in the first region of the lower part of the gate electrodes and leaving the second silicon oxide film in the second region of the lower part of the gate electrodes by isotropically

etching the second silicon oxide film, (e) a process of forming the first silicon oxide film on the top face of the semiconductor substrate and the bottom face of the gate electrodes in the first region by thermally processing the semiconductor substrate, and (f) a process of forming the second silicon nitride film on the semiconductor substrate containing a space between the first silicon oxide film formed on the top face of the semiconductor substrate and the first silicon oxide film formed on the bottom face of the gate electrodes in the first region.

[0042]

19. In Claim 17 or 18, a semiconductor integrated circuit device manufacturing method characterized by the fact that it contains a process of introducing an self-aligned impurity to the end of the first region side of the gate electrodes to form the first semiconductor region in the semiconductor substrate and a process of introducing an self-aligned impurity to the end of the second region side of the gate electrodes to form the second semiconductor region in the semiconductor substrate, and that the impurity concentration in the first semiconductor region is set lower than the impurity concentration in the second semiconductor region.

[0043]

20. In the Claim 17, 18, or 19, a semiconductor integrated circuit device manufacturing method characterized by the fact that the MISFET comprises nonvolatile memory, that gate electrodes of the MISFET comprising a peripheral circuit and gate electrodes of the MISFET comprising the nonvolatile memory are formed in a process of patterning the same conductive film, and that gate electrodes of the MISFET comprising the peripheral circuit are formed in a process of forming the second silicon oxide film.

[0044]

[Embodiments of the Invention]

Below, the embodiments of this invention are explained in detail based on the drawings. Here, in all the drawings for explaining the embodiments, the same code is used for the elements having the same function, and repetitions of the explanation are omitted.

[0045]

(Embodiment 1)

Figure 1 is an outline circuit diagram showing the main part of a flash memory (lump erasing type nonvolatile memory) which is an embodiment of this invention.

[0046]

In the memory cell array (MA) of this flash memory, are formed a plurality of word lines WL (WL1~WLm) and a plurality of source lines SL (SL1~SLm/2) extending in the right-left direction (X direction) of the figure, a plurality of bit lines DL (DL1~DLn) extending in the Y direction intersecting with them perpendicularly, and a plurality of memory cells M (M11~Mnm) configured in the MISFET structure described later.

[0047]

Each of the word lines WL (WL1~WLm) is connected to the gate electrodes of a plurality of memory cells, positioned along the X direction, and its one end is connected to a row decoder (X-DEC). Each of the source lines SL (SL1~SLm/2) is positioned as one between two word lines WL and is connected to a source common to two memory cells M neighboring in the Y direction. Also, one end of these source lines SL (SL1~SLm/2) is connected to a common source line CSL positioned in the peripheral part of the memory cell array (MA). Each of the bit lines DL (DL1~DLn) is connected to a drain common to two memory cells neighboring in the Y direction, and its one end is connected to a column decoder (Y-DEC) and a sense-up (SA).

[0048]

Figure 2 is a cross-sectional view of the main part of a semiconductor substrate showing a part of each of the memory cell array and the neighboring peripheral circuit. Fig. 3 (A) is a plan view showing a conductive layer pattern equivalent to about four memory cells, and Fig. 3 (B) is a plan view showing a conductive layer pattern equivalent to about 12 memory cells.

[0049]

A p-type well 5 is formed in a memory cell array region of a semiconductor substrate 1 made of a p-type silicon single crystal, and a p-type well 6 and an n-type well 6 are formed in the peripheral circuit region. Also, in the bottom part of the p-type well 5 in the memory cell array region, a deep n-type well 4 for separating electrically this p-type well 5 from the other regions of the semiconductor substrate is formed. On the surface of each of the p-type well 5 and the n-type well 6, is formed a field oxide film 2 made of a silicon oxide film for element separation.

[0050]

In the p-type well 5 in the memory cell array region, is formed an n-channel type MISFET Qm comprising a memory cell. Also, in the p-type well 5 in the peripheral circuit region, is formed an n-channel type MISFET Qn comprising a part of the peripheral circuit, and in the n-type well 6, is formed a p-channel type MISFET Qp comprising the other part of the peripheral circuit.

[0051]

The MISFET Qm comprising a memory cell consists mainly of a gate electrode 10a formed on a gate insulation film, an n^+-type semiconductor region 13 (drain) whose one end extends to the bottom of the gate electrode 10a, an n^+-type semiconductor region 15 (high concentration source) formed offset relative to the gate electrode 10a, an n^--type semiconductor region 11 (low concentration source) which is formed around the n^+-type semiconductor region 15 and whose one end extends to the bottom of the gate electrode 10a, and a channel formation region (p-type well 5) sandwiched by the source and drain. The gate electrode 10a is configured as one body with the word lines WL, and the source (n^+-type semiconductor region 15, n—type semiconductor region 11) is configured as one body with the source lines SL.

[0052]

The gate electrode 10a consists of, for example, a polycide film where a W (tungsten) silicide film is accumulated on the top of an n-type polycrystalline silicon film, and on its side walls are formed a side wall spacer 16 composed of a silicon oxide film. Also, a gate insulation film formed on the

bottom of the gate electrode 10a consists of one layer of silicon oxide film 9 in the drain side and three layers of insulation films where a silicon oxid film 7 and a silicon nitride film 8 are accumulated on the bottom of the silicon oxide film 9 in the source side.

[0053]

The p-channel type MISFET Qp in the peripheral circuit consists mainly of a gate electrode 10b formed on a gate insulation film (silicon oxide film 9), a pair of n^+-type semiconductor regions 14 (source and drain) formed offset relative to the gate electrode 10b, a pair of p^--type semiconductor regions 12 whose one end extends to the bottom of the gate electrode 10b, and a channel formation region (p-type well 5) sandwiched by the source and drain. Also, the n-channel type MISFET Qn in the peripheral circuit consists mainly of a gate electrode 10c formed on a gate insulation film (silicon oxide film 9), a pair of n^+-type semiconductor regions 15 (source and drain) formed offset relative to the gate electrode 10c, a pair of n^--type semiconductor regions 11 whose one end extends to the bottom of the gate electrode 10c, and a channel formation region (p-type well 5) sandwiched by the source and drain. Namely, the p-channel type MISFET Qp and the n-channel type MISFET Qn in the peripheral circuit are configured with the LDD (Lightly Doped Drain) structure. The gate electrode 10b of the p-channel type MISFET Qp and the gate electrode 10c of the n-channel type MISFT Qn are composed of polycide film in the same way as the gate electrode 10a in the memory cell, and a side wall spacer 16 composed of a silicon oxide film is formed on their side walls.

[0054]

A silicon oxide film 17 with a thick film is formed on the top of the memory cell (MISFET Qm), p-channel type MISFET Qp, and n-channel type MISFET Qn, and on its top are formed wirings 23~27 composed of an A1 alloy film for example.

[0055]

The wiring 23 formed on the memory cell array region comprises the bit lines DL and is connected to a drain (n^+-type semiconductor region 13) of the memory cell via a contact hole 20 formed on a silicon oxide film 17. Also, among the wirings 24~27 formed in the peripheral circuit region, the wirings 24 and 25 are connected to a pair of p^+-type semiconductor regions 14 (source and drain) of the p-channel type MISFET Qp via a pair of contact holes 21 formed on the silicon oxide film 17, and the wirings 26 and 27 are connected to a pair of n^+-type semiconductor regions 15 (source and drain) of the n-channel type MISFET Qn via a pair of contact holes 22 formed on the silicon oxide film 17.

[0056]

Next, the program operations of the flash memory are explained using Fig. 4 (an outline cross-sectional view showing about one memory cell), Fig. 5 (the memory cell operation voltage table), and Fig. 6 (a plot showing the potential distribution and electric field intensity distribution in the channel region at the writing operation of the memory cell).

[0057]

The writing operation sets the source (11, 15) of a selected memory cell (MISFET Qm) to the ground level (0 V) and charges the gate electrode (10a) and the drain (13) each with a positive voltage of 5 V. By this, a peak of electric field intensity shown in Fig. 6 occurs at the edge of the low concentration source (11), hot electrons (e^-) generated in this region (low concentration source side) are injected into

the electron trap inside the silicon nitride film 8, and the threshold voltage seen from the gate electrode (10a) rises, performing a writing operation.

[0058]

Also, the reading operation is performed in the same way by setting the source (11, 15) of a selected memory cell to the ground level (0 V) and charging the gate electrode (10a) and the drain (13) each with a positive voltage of 2 V. The erasing operation is performed by setting the drain (13) of a memory cell to the ground level (0 V), charging the source (11, 15) with a positive voltage of 5 V and the gate electrode (10) with a negative voltage of -10 V, respectively, and ejecting the electrons trapped in the silicon nitride film 8 to the substrate (p-type well 5) side, lowering the threshold voltage seen from the gate electrode (10a).

[0059]

Next, an example of the manufacturing method of the nonvolatile memory is explained using Fig. 7 ~ Fig. 18 (essential-section cross-sectional views of the semiconductor substrate each showing a part of the memory cell array region and its neighboring peripheral circuit region).

[0060]

First, a semiconductor substrate 1 made of a p-type silicon single crystal having a specific resistance of about 10 Ωcm is prepared as shown in Fig. 7, and after a field oxide film 2 with a film thickness of about 500 nm is formed on its surface by the selective oxidization (LOCOS) method, the semiconductor substrate 1 is thermally oxidized, forming a silicon oxide film 3 with a film thickness of about 20 nm on the surface of the element forming region surrounded with the filed oxide film 2. The silicon oxide film 3 is used as a mask when an impurity is ion implanted into the semiconductor substrate 1 in the next process.

[0061]

Next, as shown in Fig. 8, after forming a deep n-type well 4 on the semiconductor substrate 1 in the memory cell array region, a shallow p-type well 5 is formed on the semiconductor substrate 1 in the memory cell array region and a part of the peripheral circuit (n-channel type MISFET forming region), and a shallow n-type well 6 is formed on the semiconductor substrate 1 in the other part of the peripheral circuit (p-channel type MISFET forming region).

[0062]

The deep n-type well 4 is formed by ion-implanting the n-type impurity (phosphorus) to the semiconductor substrate 1 under a condition of acceleration energy 3000 keV and dose amount $1\times10^{13}/cm^2$ masked with a photoresist film with a film thickness of about 5 μm where an opening is installed in the memory cell array region. Also, the shallow p-type well 5 is formed by ion-implanting a p-type impurity (boron) to the semiconductor substrate 1 under a condition of acceleration energy 450 keV and dose amount $1\times10^{13}/cm^2$, and acceleration energy 2000 keV and dose amount $3\times10^{12}/cm^2$ masked with a photoresist film with a film thickness of about 2.5 μm where openings are installed in the memory cell array region and the n-channel type MISFET forming region. Moreover, the shallow n-type well 6 is formed by ion-implanting an n-type impurity (phosphorus) to the semiconductor substrate 1 under a condition of acceleration energy 1000 keV and dose amount $1.5\times10^{13}/cm^2$, acceleration energy 370 keV and dose amount $3\times10^{13}/cm^2$, and

acceleration energy 180 keV and dose amount $1\times10^{12}/cm^2$ masked with a photoresist film with a film thickness of about 2.5 μm where an opening is installed in the p-channel type MISFET forming region.

[0063]

Here, in the ion implantation process for forming the p-type well 5, an impurity (boron) for adjusting the threshold voltage (Vth) of the memory cell (MISFET Qm) and n-channel type MISFET Qn is ion injected at the same time (acceleration energy 50 keV, dose amount $1.2\times10^{12}/cm^2$). Also, in the ion implantation process for forming the n-type well 6, impurity (boron) for adjusting the threshold voltage (Vth) of the p-channel type MISFET Qp is ion injected at the same time (acceleration energy 20 keV, dose amount $1.5\times10^{12}/cm^2$).

[0064]

Next, after removing the silicon oxide film 3 on the surfaces of the p-type well 5 and the n-type well 6 by wet etching, as shown in Fig. 9, the semiconductor substrate 1 is thermally oxidized at about 750°C to form a silicon oxide film 7 with a film thickness of about 7 nm on the surfaces of the p-type well 5 and the n-type well 6, and further a silicon nitride film 8 with a film thickness of about 7 nm is accumulated on the top of the silicon oxide film 7 by the thermal CVD method at about 800°C.

[0065]

Next, as shown in Fig. 10, the silicon nitride film 8 and a silicon oxide film 7 are patterned to leave these films only in the source forming region of the memory cell and its vicinity. Patterning of the silicon nitride film 8 is performed by dry etching masked with a photoresist film with a film thickness of about 1 μm where openings are installed in the source forming region and its vicinity, and the patterning of the silicon oxide film 7 is performed by dry etching masked with the silicon nitride film 8 after removing the photoresist film by ashing. The widths of the two layers of insulation films (silicon oxide film 7 and silicon nitride film 8) left in the source forming region and its vicinity are adjusted so that the length of the lower portion of the gate electrode 10a (length of the longest dimension of the gate) formed in a later process becomes about 20 nm ~ 200 nm.

[0066]

Next, as shown in Fig. 11, the semiconductor substrate 1 is thermally oxidized at about 800°C to form a silicon oxide film 9 with a film thickness of about 15 nm on the surfaces of the p-type well 5 and the n-type well 6. At this time, because the silicon nitride film 8 in the memory cell array region is oxidized at the same time, a silicon oxide film 9 with a film thickness of about 2 nm is also formed on that surface.

[0067]

Next, as shown in Fig. 12, a gate electrode 10a of the memory cell (MISFET Qm) is formed on the silicon oxide film 9 in the memory cell array region, and a gate electrode 10b of the p-channel type MISFET Qn and a gate electrode 10c of the n-channel type MSFET Qp are formed on the silicon oxide film 9 in the peripheral circuit region. The gate electrodes 10a, 10b, and 10c are formed by accumulating a polycrystalline silicon film with a film thickness of about 100 nm and phosphorus concentration of about $2\times10^{20}/cm^3$ and a W silicide film with a film thickness of about 50 nm by the

thermal CVD method at about 600°C on the silicon oxide film 9, and then patterning these films by dry etching masked with a photoresist film.

[0068]

Next, as shown in Fig. 13, an n^--type semiconductor regions 11 with a low impurity concentration are formed on the p-type well 5 on both sides of each of the gate electrodes 10a and 10c and the n-type well 6 on both sides of the gate electrode 10b by ion-implanting n-type impurity (phosphorus) to the whole surface of the semiconductor substrate 1 under a condition of acceleration energy 40 keV and dose amount $1\times10^{13}/cm^2$.

[0069]

Next, as shown in Fig. 14, an n^+-type semiconductor region 13 comprising the drain of the memory cell is formed by ion-implanting an n-type impurity (arsenic) to the p-type well 5 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the drain forming region of the memory cell under a condition of acceleration energy 50 keV and dose amount $3\times10^{15}/cm^2$.

[0070]

Next, as shown in Fig. 15, a p^--type semiconductor region 12 with a low impurity concentration is formed through compensating the n^--type semiconductor region 11 to the n-type well 6 on both sides of the gate electrode 10b by ion-implanting a p-type impurity (boron difluoride) to the n-type well 6 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the p-channel type MISFET forming region under a condition of acceleration energy 50 keV and dose amount $2\times10^{13}/cm^2$.

[0071]

Next, as shown in Fig. 16, after accumulating a silicon oxide film (not shown in the figure) with a film thickness of about 200 nm on the semiconductor substrate 1 by the CVD method, a side wall spacer 16 of about 150 nm in width is formed on the side wall of each of the gate electrodes 10a, 10b, and 10c by etching anisotropically this silicon oxide film. At this time, the silicon oxide film 9 and the silicon nitride film 8 covering the source forming region of the memory cell are also etched.

[0072]

Next, as shown in Fig. 17, a p^+-type semiconductor region 14 with a high impurity concentraton comprising the source and drain of the p-channel type MISFET is formed by ion-implanting a p-type impurity (boron difluoride) to the n-type well 6 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the p-channel type MISFET forming region under a condition of acceleration energy 50 keV and dose amount $3\times10^{15}/cm^2$.

[0073]

Subsequently, an n^+-type semiconductor region 15 with a high impurity concentration comprising the source of the memory cell and an n^+-type semiconductor region 15 with a high impurity concentration comprising the source and drain of the n-channel type MISFET are formed by ion-implanting an n-type impurity (arsenic) to the p-type well 5 masked with a photoresist film with a

film thickness of about 1 μm where an opening is installed in the source forming region and the n-channel type MISFET forming region of the memory cell under a condition of acceleration energy 50 keV and dose amount $2\times10^{15}/cm^2$. Through the processes so far, the memory cell (MISFET Qm) and MISFET of the peripheral circuit (n-channel type MISFET Qn and p-channel type MISFET Qp) are completed.

[0074]

Next, as shown in Fig. 18, after accumulating a silicon oxide film 17 with a film thickness of about 500 nm on the semiconductor substrate 1 by the CVD method, contact holes 20, 21, and 22 are formed on the top of the drain of the memory cell, the top of the source and drain of the n-channel type MISFET Qn, and the top of the source and drain of the p-channel type MISFET Qp, respectively, by dry-etching the silicon oxide film 17 masked with a photoresist film.

[0075]

After that, an Al alloy film with a film thickness of about 500 nm is accumulated on the silicon oxide film 17 including the interiors of the contact holes 20~22 by the sputtering method, and wirings 23~27 are formed by patterning this Al alloy film by dry etching masked with a photoresist film, almost completing a flash memory of this embodiment shown in the Fig. 2.

[0076]

Because the flash memory of this embodiment configured in the above way has its memory cell made of a single MISFET in the same way as in the conventional floating gate type memory cell. The writing/erasing operation can be performed relatively easily, and it does not increase the necessary peripheral circuit area. Also, the manufacturing process becomes simple.

[0077]

Because the flash memory of this embodiment does not use high-resistance wiring at the reading operation such as the conventional memory cell equipped with side wall gate electrodes, no degradation in the reading speed occurs. Also, because it adopts a scheme where the gate electrode and drain are charged with a positive voltage and hot electrons generated near the source are injected to electron traps in a silicon nitride film at the writing operation, injection efficiency is improved as the potential difference between the source at the ground level and the gate electrode becomes large, enabling a lower-voltage operation than in the conventional cell structure.

[0078]

In the flash memory of this embodiment, because the gate electrodes of the memory cell cover the whole surface of the channel region, no parasitic resistance occurs immediately below the insulation film between the side wall gate electrode and the control gate electrode which is a problem in the conventional cell structure equipped with a side wall gate electrode, causing no decline in the drain current in the reading operation.

[0079]

In the flash memory manufacturing method of this embodiment, because the gate insulation film (three layers of insulation films consisting of silicon oxide film 7, silicon nitride film 8, and silicon

oxide film 9) in the source side of the memory cell is formed self-aligned to the gate electrode, it can be designed with the equivalent cell area to the conventional floating gate type memory cell, realizing nonvolatile memory excellent in scalability.

[0080]

(Embodiment 2)

A flash memory manufacturing method of this embodiment is explained using Fig. 19 ~ Fig. 33 (essential-section cross-sectional views of a semiconductor substrate each showing a part of the memory cell array region and its neighboring peripheral circuit region).

[0081]

First of all, as shown in Fig. 19, after forming a field oxide film 2 on the surface of a semiconductor substrate 1 made of a p-type silicon single crystal, a silicon oxide film 3 is formed on the surface of an element forming region surrounded with the field oxide film 2. Subsequently, after forming a deep n-type well 4 on the semiconductor substrate 1 in the memory cell array region, a shallow p-type well 5 is formed on the semiconductor substrate 1 in the memory cell array region and a part of the peripheral circuit (n-channel type MISFET forming region), and a shallow n-type well 6 is formed on the semiconductor substrate 1 in the other part of the peripheral circuit (p-channel type MISFET forming region). The processes so far are the same as in the embodiment 1.

[0082]

Next, as shown in Fig. 20, the semiconductor substrate 1 is thermally oxidized at about 800°C to form a gate oxide film 30 with a film thickness of about 15 nm on the surfaces of the p-type well 5 and the n-type well 6, afterwards as shown in Fig. 21, a polycrystalline silicon film (not shown in the figure) with a film thickness of about 200 is accumulated on the semiconductor substrate 1 by the thermal CVD method at about 600°C, and afterwards this polycrystalline silicon film 31 is dry-etched masked with a photoresist film, forming the gate electrode 31a of the memory cell and the gate electrodes 31b and 31c of the peripheral circuit.

[0083]

Next, as shown in Fig. 22, after accumulating a silicon nitride film 32 with a film thickness of about 20 nm on the semiconductor substrate 1 including the top portions of the gate electrodes 31a, 31b, and 31c by the CVD method, a silicon oxide film 33 with a film thickness of about 50 nm is accumulated on the top of the silicon nitride film 32 by the CVD method.

[0084]

Next, as shown in Fig. 23, a silicon oxide film 33 is wet-etched masked with a photoresist film with a film thickness of about 1 μm where openings are installed in the source forming region of the memory cell and its vicinity. Subsequently the photoresist film is removed by ashing, and afterwards the silicon nitride film 32 covering the source forming region of the memory cell and the gate electrode 31a in its vicinity is removed by wet-etching the silicon nitride film 32 masked with the silicon oxide film 33.

[0085]

Next, as shown in Fig. 24, the gate oxide film covering the source forming region of the memory cell is removed by wet-etching masked with the silicon nitride film 32. At this time, the gate oxide film 30 in the lower part of the gate electrode 31, a pattern-formed next to the source forming region is also etched, and a part of it is undercut over about 70 nm in width from its edge.

[0086]

Next, as shown in Fig. 25, the semiconductor substrate 1 is thermally oxidized at about 750°C to form a silicon oxide film 34 with film thickness of about 5 nm on the source forming region of the memory cell and the surface of the p-type well 5 exposed in the vicinity. At this time, the gate electrode 31a exposed in the vicinity of the source forming region of the memory cell, is also oxidized at the same time, forming a silicon oxide film 35 with film thickness of about 5 nm on its surface.

[0087]

Next, as shown in Fig. 26, a silicon nitride film 36 with film thickness of about 10 nm is accumulated on the semiconductor substrate 1 by the CVD method. By this, three layers of gate insulation film consisting of the silicon oxide film 34, silicon nitride film 36, and silicon oxide film 35 are formed in the source forming region side in the lower part of the gate electrode 10a.

[0088]

Next, as shown in Fig. 27, the n^--type semiconductor regions 37 with a low impurity concentration are formed on the p-type well 5 on both sides of each of the gate electrodes 10a and 10c and the n-type well 6 on both sides of the gate electrode 10b by ion-implanting a n-type impurity (phosphorus) to the whole surface of the semiconductor substrate 1 under a condition of acceleration energy 40 keV and dose amount $1\times10^{13}/cm^2$.

[0089]

Next, as shown in Fig. 28, an n^+-type semiconductor region 39 comprising the drain of the memory cell is formed by ion-implanting a n-type impurity (arsenic) to the p-type well 5 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the drain forming region of the memory cell under a condition of acceleration energy 50 keV and dose amount $3\times10^{15}/cm^2$.

[0090]

Next, as shown in Fig. 29, a p^--type semiconductor region 38 with a low impurity concentration is formed through compensating the n^--type semiconductor region 37 to the n-type well 6 on both sides of the gate electrode 31b by ion-implanting a p-type impurity (boron difluoride) to the n-type well 6 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the p-channel type MISFET forming region under a condition of acceleration energy 50 keV and dose amount $2\times10^{13}/cm^2$.

[0091]

Next, as shown in Fig. 30, after accumulating a silicon oxide film with a film thickness of about 200 nm on the semiconductor substrate 1 by the CVD method, a side wall spacer 42 of about 150 nm in

width is formed on side wall of each of the gate electrodes 31a, 31b, and 31c by etching anisotropically this silicon oxide film. At this time, the silicon oxide film 35 and the silicon nitride film 36 covering the upper parts of the gate electrodes 31a, 31b, and 31c are also etched at the same time, exposing the surfaces of the gate electrodes 31a, 31b, and 31c.

[0092]

Next, as shown in Fig. 31, a p^+-type semiconductor region 40 with a high impurity concentration comprising the source and drain of the p-channel type MISFET is formed by ion-implanting a p-type impurity (boron difluoride) to the n-type well 6 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the p-channel type MISFET forming region under a condition of acceleration energy 50 keV and dose amount $3\times10^{15}/cm^2$.

[0093]

Subsequently, an n^+-type semiconductor region 41 with a high impurity concentration comprising the source of the memory cell and an n^+-type semiconductor region 41 with a high impurity concentration comprising the source and drain of the n-channel type MISFET are formed by an ion-implanting n-type impurity (arsenic) to the p-type well 5 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the source forming region and the n-channel type MISFET forming region of the memory cell under a condition of acceleration energy 50 keV and dose amount $2\times10^{15}/cm^2$. Through the processes so far, the memory cell (MISFET Qm) and MISFET of the peripheral circuit (n-channel type MISFET Qn and p-channel type MISFET Qp) are completed.

[0094]

Next, after removing he silicon oxide film 34 covering the surfaces of the source and drain of the MISFET by etching the surface of the semiconductor substrate 1, as shown in Fig. 32, silicide layers 43 of low resistance are formed on the surfaces of the gate electrodes 31a, 31b, and 31c and the source and drain (n^+-type semiconductor region 39, p^+-type semiconductor region 40, and n^+-type semiconductor region 41). The silicide layer 43 is formed, for example, by accumulating a high melting point metal film such as Co (cobalt) film and Ti (cobalt) film by the sputtering method, next thermally processing the semiconductor substrate 1 to react the high melting point metal film with the substrate (Si) and the gate electrodes (31a~31c) forming a Co silicide layer, and removing the unreacted high melting point metal film by wet etching.

[0095]

Next, as shown in Fig. 33, in the same way as in embodiment 1, after forming contact holes 45, 46, and 47 on a silicon oxide film 44 accumulated on the semiconductor substrate 1, wirings 48~52 are formed on the top of the silicon oxide film 44, almost completing the flash memory of this embodiment 2.

[0096]

Figure 34 is a table listing the photomasks used in the manufacturing method. Among the thirteen photomasks used in the metal manufacturing process, the photomasks proper to manufacture memory cell are two pieces of one (No. 6) for processing silicon nitride film and another (No. 7) for drain formation, being very simplified.

[0097]

Also, the writing/erasing operation property and retention property of the flash memory manufactured in the method were in the same degrees with those of the flash memory of the embodiment 1.

[0098]

(Embodiment 3)

Figure 35 is an essential-section cross-sectional view of a semiconductor substrate showing the cell structure of a flash memory of this embodiment.

[0099]

While the drain-side gate insulation film is composed of one layer of silicon oxide film 9 in the memory cell (MISFET Qm) of embodiment 1, in this embodiment the drain-side gate insulation film is composed of two layers of the silicon oxide film 9 and silicon oxide film 60 formed underneath. Also, the electric capacity film thickness of the drain-side gate insulation film consisting of these two layers of silicon oxide film 9 and 60 is approximately equal to the electric capacity film thickness of the source-side gate insulation film composed of the silicon oxide film 7 and 9 and a silicon nitride film 8 sandwiched between them. Namely, the gate insulation film of this memory cell consists of almost the same electric capacity film thickness (about 17.5 nm for example) in the drain side and source side.

[0100]

The configuration and program operation of the memory cell of this embodiment, except as described above, are the same as those of the memory cell of embodiment 1. Also, the memory cell manufacturing method of this embodiment is the same as the manufacturing method in embodiment 1, except that one process increases, where the silicon oxide film 60 is formed by thermally processing the semiconductor substrate 1.

[0101]

According to the flash memory of this embodiment, by setting the electric capacity film thickness of the gate insulation film about the same over the entire lower part of the gate electrode 10a, even when the length of the source-side gate insulation film (silicon oxide film 9, silicon nitride film 8, and silicon oxide 7) along the gate length direction varies due to a variation in the manufacturing process, the drain current driving capability will not change. By this, because the drain current at the writing operation becomes constant, a variation of writing time is prevented, and a stable memory cell property becomes possible.

[0102]

(Embodiment 4)

Figure 36 is an essential-section cross-sectional view of a semiconductor substrate showing the cell structure of a flash memory of this embodiment.

[0103]

While only the source-side gate insulation film is composed of a three-layer film (silicon oxide film 9, silicon nitride film 8, and silicon oxide film 7), in this embodiment the whole drain-side gate insulation film in the lower part of the gate electrode 10a is composed of the three-layer film (silicon oxide film 9, silicon nitride film 8, and silicon oxide film 7). The film thickness of these three layers total about 7 nm.

[0104]
The configuration and program operation of the memory cell of this embodiment other than those differences described above are the same as the memory cell of embodiment 1. Also, the memory cell manufacturing method of this embodiment is the same as the manufacturing method described in embodiment 1, except that one process is omitted where the silicon oxide film 7 and silicon nitride film 8 are patterned to leave them only in the source side. This memory cell was written at 1 μ/sec.

[0105]

(Embodiment 5)

Figure 37 is an essential-section cross-sectional view of a semiconductor substrate showing the cell structure of a flash memory of this embodiment.

[0106]

This flash memory cell is composed with the MISFET Qc which is a memory element section and the selection MISFET Qs. The MISFET Qc in the memory element section mainly consists of a writing/erasing gate electrode (PEG) 73 made of a polycrystallne silicon film formed on a gate insulation film with three-layer structure consisting of a bottom gate oxide film 70 with a film thickness of about 8 nm, a silicon nitride film 71 with a film thickness of about 10 nm, and a top gate oxide film 72 with a film thickness of about 10 nm, etc. and a source and a drain (connecting diffusion layer) formed on a semiconductor substrate 1 on both sides of this gate electrode 73.

[0107]

The source consists of an n^--type semiconductor region 74 with a low impurity concentration whose one end extends to the bottom of the gate electrode 73 and an n^+-type semiconductor region with a high impurity concentration formed so that it is offset relative to the gate electrode 73, and the drain (connecting diffusion layer) consists of an n^+-type semiconductor region 76 whose one end extends to the bottom of the gate electrode 73.

[0108]

Also, the selection MISFET Qs mainly consists of a selection gate electrode (SG) 78 made of a polycrystalline silicon film etc. formed on the top of the gate oxide film 77 with a film thickness of about 4 nm, a source (connecting diffusion layer) and a drain formed on the semiconductor substrate 1 on both sides of this gate electrode 78. The drain consists of an n^--type semiconductor region 79 with a high impurity concentration whose one end extends to the bottom of the gate electrode 78. The source consists of an n^+-type semiconductor region 76 which is the drain of the MISFET Qc, and its one end extends to the bottom of the gate electrode 78.

[0109]

The program operations of the flash memory is explained using Fig. 38 (a memory cell operation voltage table). Writing is performed by charging the drain of the selection MISFET Qs with 5 V, the gate electrode 78 with 2 V, turning the selection MISFET Qs on, charging the gate electrode 73 with 5 V with the source of the MISFET Qc of the memory element section as the ground level (0 V), and a peak in the electric field intensity is generated near an n^--type semiconductor region 74 with a low impurity concentration comprising a part of the source. By this, hot electrons generated in this region are injected to the electron traps inside the silicon nitride film 71, the threshold voltage seen from the gate electrode 73 of the MISFET Qc rises to 4 V or higher, and writing is performed. Because this memory cell can control the drain current with the voltage charged to the gate electrode 73, compared with the conventional MNOS-type memory cell where electrons are injected to the whole surface of a silicon nitride film from the substrate side via a direct tunnel oxide film by controlling the potential of the substrate and writing/erasing gate electrode, writing can be performed with lower electric power consumption.

[0110]

The erasing operation is performed by charging the gate electrode 73 of the MISFET Qc with −10 V and the source and well with 5 V, and ejecting electrons inside the silicon nitride film 71. Also, the writing operation is performed by charging the drain gate electrode 73 of the selection MISFET Qs and the gate electrode 73 of the MISFET Qc with 2 V, and judging the threshold voltage of the MISFET Qc.

[0111]

(Embodiment 6)

Figure 39 is an essential-section cross-sectional view of a semiconductor substrate showing the cell structure of a flash memory of this embodiment.

[0112]

The MISFET comprising this memory cell mainly consists of a gate electrode 83 made of a polycrystalline silicon film etc. formed on a gate insulation film, and a source and a drain formed on a semiconductor substrate 1 on both sides of this gate electrode 83. The source consists of an n^+-type semiconductor region 84 with a high impurity concentration whose one end extends to the lower part of the gate electrode 83, and the drain consists of a p^--type semiconductor region 85 with a low impurity concentration (about 1×10^{18}~$10^{19}/cm^3$) whose one end extends to the lower part of the gate electrode 83 and an n^+-type semiconductor region 86 with a high impurity concentration formed offset relative to the gate electrode 83. Also, in the gate insulation film, while the source side consists of a gate oxide 82 with a film thickness of about 10 nm, the drain size consists of a bottom gate oxide film 80 with a film thickness of about 8 nm, a silicon nitride film 81 with a film thickness of about 10 nm, and a top gate oxide film 82 with a film thickness of about 10 nm. In this way, the memory cell of this embodiment has a characteristic in that it performs the injection of hot electrons at the time of writing in the drain side.

[0113]

As shown in Fig. 40, the writing and erasing operations of this flash memory are the same as in the memory cell of embodiment 1. On the other hand, writing is performed by charging each of the gate electrode 83 and the source with a positive voltage of 5 V with the drain of the selected memory cell as the ground level (0 V).

[0114]

Figure 41 is a plot showing time change of the voltage charged to each terminal at the writing operation. Writing is performed by pre-charging all the bit lines to 5 V after charging the common source line of the selected memory block with 5 V. Next, after raising the potential of only the selected word line to 5 V, only the selected bit line is lowered to 0 V. This time for lowering it to 0 V is the writing time, and a channel current flows from the source to drain direction of the memory cell within this time. At this time, as shown in Fig. 42, because most of the potential levels set to 5 V in the source side and 0 V in the drain side drop in the low concentration drain (p^--type semiconductor region 85) region, a peak of the electric field intensity occurs at the edge of the drain. Then, hot electrons generated by this high electric field are accelerated by the transverse direction electric field of 5 V charged to the selected word line and injected to the electron traps inside the silicon nitride film 81, thus performing writing.

[0115]

(Embodiment 7)

Figure 43 is an essential-section cross-sectional view of a semiconductor substrate showing the cell structure of a flash memory of this embodiment.

[0116]

This memory cell performs the injection of hot electrons at the writing time in the drain side and has the same cell structure as embodiment 6 except that the source consists of an n^--type semiconductor region 87 with a low impurity concentration whose one end extends to the lower part of the gate electrode 83 and an n^+-type semiconductor region 84 with a high impurity concentration formed offset relative to the gate electrode 83.

[0117]

Writing is started by pre-charging all the bit lines to 5 V after charging the common source line of the selected memory block to 5 V in the same way as embodiment 6. By the way, if this 5 V power supply for writing is an internal power supply such as a booster circuit formed on a chip, because the power supply capability is limited, there occurs a problem that charging to a large enough voltage becomes impossible if there is a large connection leak of the current of the common source line to be charged. In this embodiment, by forming an n^--type semiconductor region 87 with a low impurity concentration in the source side, because the electric field of the source connection is moderated when charging the source at the writing time. The problem can be avoided by attempting a reduction of the leak current and an improvement of the connection voltage resistance of the source connection.

[0118]

(Embodiment 8)

Figure 44 is an outline plan showing the cell structure of a flash memory of this embodiment, and Fig. 45 is a essential-section cross-sectional view of the semiconductor substrate along the A-A' line in Fig. 44.

[0119]

In the MISFET Qm comprising the memory cell of this embodiment, in the same way as embodiment 1, the source-side gate insulation film consists of a three-layer film (silicon oxide film 9, silicon nitride film 8, and silicon oxide film 7), and the drain side consists of a one layer of silicon oxide film 9. On the other hand, the bit lines DL and the drain (n^+-type semiconductor region 92) are electrically connected via a plug 98 formed on the upper part of the drain. Also, the sources (n^+-type semiconductor region 92) of a plurality of memory cells along the extending direction of the gate electrode 90 are electrically connected via the source lines (SL) consisting of plug 98 formed on their top.

[0120]

In order to manufacture the memory cell, first as shown in Fig. 46, after a deep n-type well 4 and a shallow p-type well 5 are formed on a p-type semiconductor substrate 1 by the same method as in embodiment 1, a gate insulation film whose source side consists of a three-layer film (silicon oxide film 9, silicon nitride film 8, and silicon oxide film 7) and drain side consists of one layer of silicon oxide film 9 is formed on the surface of the p-type well 5.

[0121]

The silicon oxide film 7 is formed by thermally oxidizing the semiconductor substrate 1 at about 800°C, and its film thickness is set to about 11 nm. Also, the silicon nitride film 8 is formed by the thermal CVD method at about 730°C, and its film thickness is set to about 10 nm. Moreover, the silicon oxide film 9 is formed by patterning the silicon nitride film 8 and silicon oxide film 7 to leave these films only on the source forming region of the memory cell and its vicinity, and then thermally oxidizing the semiconductor substrate 1 at about 800°C, and its film thickness is set to about 15 nm.

[0122]

Next, as shown in Fig. 47, a polycrystalline silicon film with a film thickness of about 100 nm and phosphorus concentration of about $2\times10^{20}/cm^3$ is accumulated on the top of the silicon oxide film 9 by the CVD method, and next after accumulating a silicon nitride film 93 with a film thickness of about 200 nm on the top by the CVD method, these films are patterned by dry etching masked with a photoresist film, forming a gate electrode 90 consisting of the polycrystalline silicon film.

[0123]

Next, as shown in Fig. 48, a p^--type semiconductor region 91 is formed by ion-implanting a p-type impurity (boron) to the p-type well 5 from an oblique 30° angle masked with a photoresist film where an opening is installed in the source forming region under a condition of acceleration energy 20 keV and dose amount $1\times10^{13}/cm^2$. Subsequently, an n+-type semiconductor region 92 comprising the source and drain is formed on the p-type well 5 on both sides of the gate electrode 90 by an ion-implanting n-type impurity (arsenic) to the whole surface of the memory cell array region under a condition of acceleration energy 50 keV and dose amount $2\times10^{15}/cm^2$.

[0124]

Next, as shown in Fig. 49, after accumulating a silicon nitride film on the semiconductor substrate 1 by the CVD method, by anisotropically etching this silicon nitride film, a side wall spacer 94 is formed on the side wall of the gate electrode 90. At this time, the gate insulation film covering the surfaces of the source and drain is etched at the same time.

[0125]

Next, as shown in Fig. 50, after accumulating a silicon oxide film 95 on the semiconductor substrate 1 by the CVD method, by etching this silicon oxide film 95 masked with a photoresist film where an opening is installed on the upper part of the drain, a contact hole 96 is formed in the source line forming region including the upper part of the source, and a contact hole 97 is formed on the upper part of the drain.

[0126]

In the process of etching the silicon oxide film 95, because the side wall spacer 94 of silicon nitride formed on the side wall, the gate electrode 90 functions as an etching stopper, the contact holes 96 and 97 are formed self-aligned to the space of the gate electrode 90. By this, because the fitting allowance between the contact holes 96 and 97 and the gate electrode 90 becomes unnecessary, the space of the gate electrode 90 can be designed in the minimum processing size.

[0127]

Next, as shown in Fig. 91, source lines (SL) are formed inside the contact hole 96, and a plug 98 is formed inside the contact hole 97. The source lines (SL) and the plug 98 are formed by accumulating a polycrystalline silicon film doped with an n-type impurity on the top of the silicon oxide film 95 by the CVD method and then flattening the surface of this polycrystalline silicon film by the chemical-mechanical polishing (CMP) method.

[0128]

Subsequently, after accumulating a silicon oxide film 99 on the top of the silicon oxide film 95 by the CVD method, an Al alloy film is accumulated on the top of the silicon oxide film 99 by the sputtering method, and by patterning this Al alloy film by dry etching masked with a photoresist film to form bit lines DL, the flash memory of this embodiment shown in the Fig. 44 and Fig. 45 is almost completed.

[0129]

According to this embodiment, because the space of the gate electrode 90 can be designed with the minimum processing size, the cell area could be reduced to 0.5 $\mu m \times 0.4\ \mu m = 0.2\ \mu m^2$ at the gate length of 0.3 μm. Also, writing time of the memory cell was 5 microseconds and the erasing time was 10 milliseconds, confirming enough stable retention property similar to the embodiment 1.

[0130]

Above, although the invention made by the present inventors was explained concretely based on the embodiments, this invention is not limited to the embodiments but can be changed in various ways within the range not deviating from its essence.

[0131]

Because the nonvolatile memory of this invention has a simple cell structure and a simple manufacturing process, application to LSIs where nonvolatile memory and logic LSI are mounted on the same semiconductor substrate is also easy.

[0132]

[Efficacy of the Invention]

Among the inventions disclosed in this application, the effects obtained by the representative ones are simply explained below.

[0133]

In the nonvolatile memory of this invention, because the memory cell consists of a single MISFET, writing/erasing operation can be performed relatively easily, not increasing the necessary peripheral circuit area. Also, its manufacturing process is simple.

[0134]

Because the nonvolatile memory of this invention adopts a scheme where a positive voltage is charged to the gate electrode and drain at the writing operation and hot electrons generated near the source are injected to the electron traps inside the silicon nitride film, the potential difference between the source at the ground level and the gate electrode becomes large, improving the injection efficiency and enabling operation at a lower voltage compared with the conventional cell structure.

[0135]

In the nonvolatile memory manufacturing method of this invention, because the source-side gate insulation film (a three-layer insulation film consisting of silicon oxide film, silicon nitride film, and silicon oxide film) of the memory cell is formed self-aligned to the gate electrode, it can be designed to have the equivalent cell area to the conventional floating gate type memory cell, realizing nonvolatile memory excellent in scalability.

[Brief Explanation of the Drawings]

[Fig. 1]

An outline circuit diagram showing the main section of the flash memory which is embodiment 1 of this invention.

[Fig. 2]

A cross-sectional view showing the essential section of the flash memory which is embodiment 1 of this invention.

[Fig. 3A]

A plan view showing the conductive layer pattern of the flash memory which is embodiment 1 of this invention.

[Fig. 3B]

A plan view showing the conductive layer pattern of the flash memory which is embodiment 1 of this invention.

[Fig. 4]

An outline cross-sectional view explaining the program operation of the flash memory which is embodiment 1 of this invention.

[Fig. 5]

An operation voltage table explaining the program operation of the flash memory which is embodiment 1 of this invention.

[Fig. 6]

A plot showing the potential distribution and electric field intensity distribution in the channel region in the writing operation of the flash memory which is embodiment 1 of this invention.

[Fig. 7]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 8]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 9]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 10]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 11]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 12]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 13]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 14]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 15]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 16]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 17]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 18]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 19]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 20]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 21]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 22]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 23]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 24]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 25]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 26]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 27]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 28]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 29]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 30]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 31]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 32]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 33]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 34]

A flow chart showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 35]

An outline cross-sectional view of the flash memory which is embodiment 3 of this invention.

[Fig. 36]

An outline cross-sectional view of the flash memory which is embodiment 4 of this invention.

[Fig. 37]

An outline cross-sectional view of the flash memory which is embodiment 5 of this invention.

[Fig. 38]

An operation voltage table explaining the program operation of the flash memory which is embodiment 5 of this invention.

[Fig. 39]

An outline cross-sectional view of the flash memory which is embodiment 6 of this invention.

[Fig. 40]

An operation voltage table explaining the program operation of the flash memory which is embodiment 6 of this invention.

[Fig. 41]

A plot showing the time change of charged voltage in the writing operation of the flash memory which is embodiment 6 of this invention.

[Fig. 42]

A plot showing the potential distribution and electric field intensity distribution of the channel region in the writing operation of the flash memory which is embodiment 6 of this invention.

[Fig. 43]

An outline cross-sectional view of the flash memory which is embodiment 7 of this invention.

[Fig. 44]

An essential-section cross-sectional view showing the cell structure of the flash memory which is embodiment 8 of this invention.

[Fig. 45]

An essential-section cross-sectional view of the semiconductor substrate along the A-A' line in Fig. 44.

[Fig. 46]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 47]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 48]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 49]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 50]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 51]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 52]

An outline cross-sectional view showing the cell structure of a floating gate type memory cell.

[Fig. 53]

An outline cross-sectional view showing the cell structure of an MNOS-type memory cell.

[Fig. 54]

An outline cross-sectional view showing the cell structure of a memory cell having a selection gate electrode and a side wall gate electrode.

[Fig. 55]

A plot showing the potential distribution and electric field intensity distribution of the channel region in the writing operation of the flash memory shown in Fig. 54.

[Explanation of the Codes]

1: Semiconductor substrate
2: Field oxide film
3: Silicon oxide film
4: (Deep) n-type well
5: p-type well
6: n-type well
7: Silicon oxide film
8: Silicon nitride film
9: Silicon oxide film
10a, 10b, 10c: Gate electrodes
11: n^--type semiconductor region
12: p^--type semiconductor region
13: n^+-type semiconductor region
14: p^+-type semiconductor region
15: n^+-type semiconductor region
16: Side wall spacer
17: Silicon oxide film
20~22: Contact holes
23~27: Wirings
30: Gate oxide film
31a, 31b, 31c: Gate electrodes
32: Silicon nitride film
33: Silicon oxide film
34: Silicon oxide film
35: Silicon oxide film
36: Silicon nitride film
37: n^--type semiconductor region
38: p^--type semiconductor region
39: n^+-type semiconductor region
40: p^+-type semiconductor region
41: n^+-type semiconductor region
42: Side wall spacer

43: Silicide film
44: Silicon oxide film
45~47: Contact holes
48~52: Wiring 60 Silicon oxide film
70: Bottom gate oxide film
71: Silicon nitride film
72: Top gate oxide film
73: Gate electrode
74: n^--type semiconductor region
75: n^+-type semiconductor region
76: n^+-type semiconductor region
77: Gate oxide film
78: Gate electrode
79: n^+-type semiconductor region
80: Bottom gate oxide film
81: Silicon nitride film
82: (Top) Gate oxide film
83: Gate electrode
84: n^--type semiconductor region
85: p^--type semiconductor region
86: n^+-type semiconductor region
87: n^--type semiconductor region
90: Gate electrode
91: p^--type semiconductor region
92: n^+-type semiconductor region (source, drain)
93: Silicon nitride film (cap)
94: Side wall spacer
95: Silicon oxide film
96, 97: Contact holes
98: Plug
99: Silicon oxide film
101: Silicon substrate
102: Gate oxide film
103: Floating gate
104: Interlayer insulation film
105: Control gate
106: Source
107: Drain
108: Electron
111: Silicon substrate
112: Direct tunnel oxide film
113: Silicon nitride film
114: Gate oxide film
115a, 115b: Gate electrode
116: Source
117: Connecting diffusion layer drain
118: Gate oxide film
119: Drain
121: Silicon substrate
122: Gate oxide film

123: Selection gate electrode
124: Silicon oxide film
125: Silicon nitride film
126: Silicon oxide film
127: Side wall gate electrode
128: Source
129: Drain
CSL: Common source line
DL (DL1~DLn): Bit lines
MA: Memory cell array
M (M11~Mnm): Memory cells
Qc: MISFET
Qm: MISFET
Qs: Selection MISFET
SL (SL1~SLm/2): Source lines
SA: Sense amplifier
WL (WL1~WLm): Word lines
X-DEC: Low decoder
Y-DEC: Column decoder

[Abstract]

[Objective]

The objective of this invention is to provide a nonvolatile memory equipped with a new cell structure having both scalability comparable to the floating gate type memory cell and reliability equivalent to or higher than the MNOS-type memory cell and its manufacturing method.

[Resolution Means]

The MISFET Qm comprising nonvolatile memory consists of a gate electrode 10a formed on the gate insulation film, an n^+-type semiconductor region 13 (drain) whose one end extends to the bottom of a gate electrode 10a, an n^+-type semiconductor region 15 (high concentration source) formed offset relative to the gate electrode 10a, and an n^--type semiconductor region 11 (low concentration source) whose one end extends to the bottom of the gate electrode 10a. In the gate insulation film, the drain side consists of one layer of silicon oxide film 9, the source side consists of three layers of insulation films where a silicon oxide film 7, a silicon nitride film 8, and a silicon oxide film 9 are accumulated.

[Fig. 5]

Terminal	Bit lines (Drain voltage)		Word lines (Gate voltage)		Source lines	Well
	Select	Deselect	Select	Deselect		
Write	5 V	0 V	5 V	0 V	0 V	0 V
Erase	0 V	0 V	-10 V	0 V	5 V	5 V
Read	2 V	0 V	2 V	0 V	0 V	0 V

[Fig. 34]
1. Isolation formation
2. Deep n-type well implantation
3. Shallow n-type well implantation

4. p^--type well implantation
5. Gate electrode processing
8. Peripheral pMOS low concentration source & drain implantation
9. n^+-type semiconductor region implantation
10. p^+-type semiconductor region implantation
11. Contact hole opening
12. First metal wiring processing

[Fig. 38]

Terminal	Bit lines (D)		Word lines (SG)		Write/Erase lines (PEG)		Source lines (S)	Well
	Select	Deselect	Select	Deselect	Select	Deselect		
Write	5 V	0 V	2 V	0 V	5 V	0 V	0 V	0 V
Erase	0 V	0 V	0 V	0 V	-10 V	0 V	5 V	5 V
Read	2 V	0 V	2 V	0 V	2 V	0 V	0 V	0 V

[Fig. 40]

Terminal	Bit lines (Drain voltage)		Word lines (Gate voltage)		Source lines	Well
	Select	Deselect	Select	Deselect		
Write	0 V	5 V	5 V	0 V	5 V	0 V
Erase	0 V	0 V	-10 V	0 V	5 V	5 V
Read	2 V	0 V	2 V	0 V	0 V	0 V

Continued from the front page

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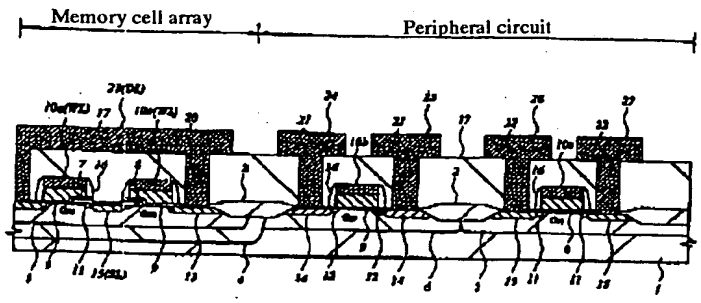
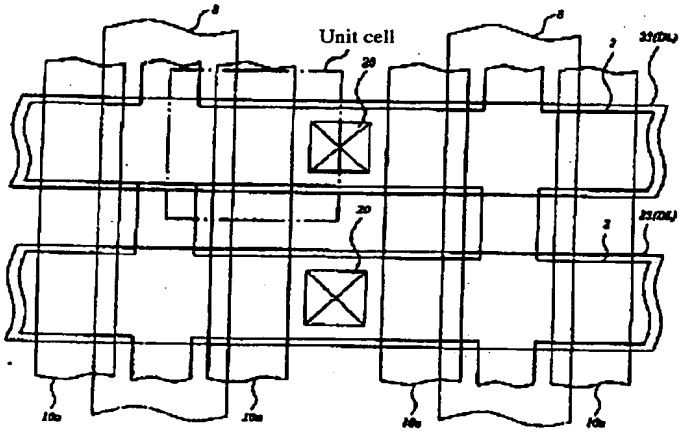
(58) Investigated Fields (Int. Cl.[6], DB name)

H01L 27/115
H01L 21/8247
H01L 29/788
H01L 29/792

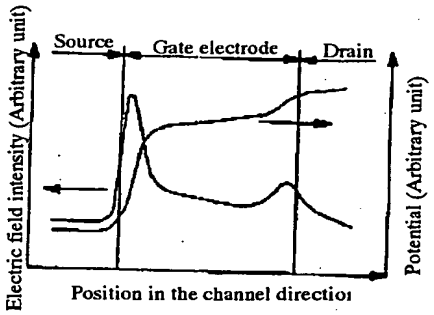
[Fig. 2]

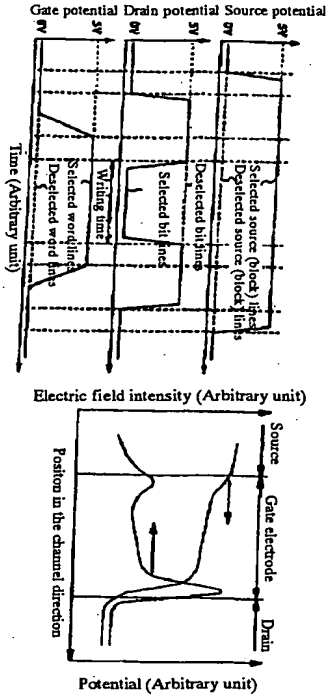


[Fig. 3A]



[Fig. 6]


Source
Gate electrode
Drain
Electric field intensity (Arbitrary unit)
Potential (Arbitrary unit)
Position in the channel direction

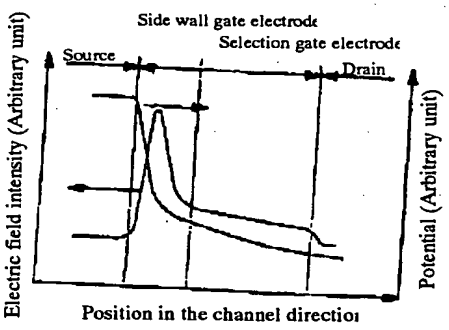

Gate potential
Drain potential
Source potential
5V
0V
Time (Arbitrary unit)
Deselected word lines
Selected wordline
Writing time
Selected bit lines
Deselected bit lines
Selected source (block) lines
Deselected source (block) lines

[Fig. 41]

Electric field intensity (Arbitrary unit)
Position in the channel direction
Source
Gate electrode
Drain
Potential (Arbitrary unit)

[Fig. 42]

[Fig. 55]


Side wall gate electrode
Selection gate electrode
Source
Drain
Electric field intensity (Arbitrary unit)
Potential (Arbitrary unit)
Position in the channel direction

1. JP,2978477,B

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

---

(57) [Claim(s)]
[Claim 1] A gate electrode connected to a word line and an electric target is formed on a gate insulator layer formed on a semiconductor substrate of the 1st conductivity type. The 1st and 2nd semiconductor region of the 2nd conductivity type which constitutes the source and a drain is formed in said semiconductor substrate. It is semiconductor integrated circuit equipment with which a memory cell of a non-volatile was constituted by MISFET by which a channel field is formed between said 1st semiconductor region and said 2nd semiconductor region. Said 1st semiconductor region side at least said gate insulator layer The 1st silicon oxide film, It is semiconductor integrated circuit equipment characterized by consisting of an insulator layer of three layers which carried out the laminating of a silicon nitride film and the 2nd silicon oxide film, and carrying out by writing of said memory cell making said 2nd semiconductor region high potential rather than said 1st semiconductor region.
[Claim 2] A gate electrode connected to a word line and an electric target is formed on a gate insulator layer formed on a semiconductor substrate. The 1st and 2nd semiconductor region of the 2nd conductivity type which constitutes the source and a drain is formed in said semiconductor substrate. It is semiconductor integrated circuit equipment with which a memory cell of a non-volatile was constituted by MISFET by which a channel field is formed between said 1st semiconductor region and said 2nd semiconductor region. Said 1st semiconductor region side at least said gate insulator layer The 1st silicon oxide film, High impurity concentration of a portion which consists of an insulator layer of three layers which carried out the laminating of a silicon nitride film and the 2nd silicon oxide film, and extends in the lower part of said gate electrode of said 1st semiconductor region Semiconductor integrated circuit equipment characterized by pouring said hot electron into said silicon nitride film by being lower than high impurity concentration of a portion which extends in the lower part of said gate electrode of said 2nd semiconductor region, and generating a hot electron in said 1st semiconductor region side.
[Claim 3] A gate electrode connected to a word line and an electric target is formed on a gate insulator layer formed on a semiconductor substrate. The 1st and 2nd semiconductor region of the 2nd conductivity type which constitutes the source and a drain is formed in said semiconductor substrate. It is semiconductor integrated circuit equipment with which a memory cell of a non-volatile was constituted by MISFET by which a channel field is formed between said 1st semiconductor region and said 2nd semiconductor region. Said 1st semiconductor region side said gate insulator layer The 1st silicon oxide film, It consists of an insulator layer of three layers which carried out the laminating of a silicon nitride film and the 2nd silicon oxide film. High impurity concentration of a portion to which said 2nd semiconductor region side extends in the lower part of said gate electrode of said 1st semiconductor region by consisting of a silicon oxide film is semiconductor integrated circuit equipment characterized by differing from high impurity concentration of a portion which extends in the lower part of said gate electrode of said 2nd semiconductor region.
[Claim 4] High impurity concentration of a portion which is semiconductor integrated circuit equipment according to claim 1 or 3, and extends in the lower part of said gate electrode of said 1st semiconductor region is semiconductor integrated circuit equipment characterized by being lower than high impurity concentration of a portion which extends in the lower part of said gate electrode of said 2nd semiconductor region.
[Claim 5] It is semiconductor integrated circuit equipment which is semiconductor integrated circuit equipment according to claim 1, 2, or 4, and is characterized by for said gate insulator layer consisting of an insulator layer of three layers to which said 1st semiconductor region side carried out the laminating of said 1st silicon oxide film, a silicon nitride film, and the 2nd silicon oxide film, and said 2nd semiconductor region side consisting of a silicon oxide film.
[Claim 6] It is semiconductor integrated circuit equipment characterized by being semiconductor integrated circuit equipment given in any 1 term of claims 1-5, and said gate insulator layer having the electric capacity thickness with almost same said 1st semiconductor region side and said 2nd semiconductor region side.
[Claim 7] It is semiconductor integrated circuit equipment characterized by being semiconductor integrated circuit

equipment according to claim 1, 2, 4, 5, or 6, and said gate insulator layer consisting of an insulator layer of three layers to which said said 1st semiconductor region and 2nd semiconductor region side carried out the laminating of said 1st silicon oxide film, a silicon nitride film, and the 2nd silicon oxide film.

[Claim 8] It is semiconductor integrated circuit equipment which is semiconductor integrated circuit equipment according to claim 1, 3, 4, 5, 6, or 7, and is characterized by performing writing of said memory cell by pouring in a hot electron into said silicon nitride film which constitutes said a part of gate insulator layer.

[Claim 9] Thickness of said 1st silicon oxide film which is semiconductor integrated circuit equipment given in any 1 term of claims 1-8, and was formed in a lower layer of said silicon nitride film among said insulator layers of three layers which constitute said a part of gate insulator layer [at least] is semiconductor integrated circuit equipment characterized by being thicker than thickness to which direct tunnel current flows.

[Claim 10] It is semiconductor integrated circuit equipment which it is semiconductor integrated circuit equipment given in any 1 term of claims 1-9, and said 2nd semiconductor region consists of a semiconductor region of the 1st conductivity type with which the end extends in the lower part of said gate electrode, and a semiconductor region of the 2nd conductivity type which the end estranged from said gate electrode, and is characterized by said 1st semiconductor region consisting of the 2nd conductivity type.

[Claim 11] It is semiconductor integrated circuit equipment which is semiconductor integrated circuit equipment given in any 1 term of claims 1-10, and is characterized by making read-out of said memory cell into high potential, and performing said 1st semiconductor region rather than said 2nd semiconductor region.

[Claim 12] It is semiconductor integrated circuit equipment which is semiconductor integrated circuit equipment given in any 1 term of claims 1-10, and is characterized by making read-out of said memory cell into high potential, and performing said 2nd semiconductor region rather than said 1st semiconductor region.

[Claim 13] It is semiconductor integrated circuit equipment given in any 1 term of claims 1-12. A source line is formed of a plug embedded at the 1st connection hole formed in an insulator layer of one upper part of said 1st and 2nd semiconductor region. Semiconductor integrated circuit equipment characterized by connecting a bit line to another side of said 1st and 2nd semiconductor region through a plug embedded at the 2nd connection hole formed in said insulator layer of the upper part of another side of said 1st and 2nd semiconductor region.

[Claim 14] It is semiconductor integrated circuit equipment characterized by being semiconductor integrated circuit equipment according to claim 13, and forming said 1st connection hole and said 2nd connection hole by self align to a space of a gate electrode of said MISFET.

[Claim 15] It is semiconductor integrated circuit equipment characterized by being semiconductor integrated circuit equipment given in any 1 term of claims 1-14, and said memory cell consisting of said MISFET which constitutes the storage element section, and MISFET for selection.

[Claim 16] It is semiconductor integrated circuit equipment which is semiconductor integrated circuit equipment given in claims 1-9 and any 1 term of 11-15, and is characterized by said 1st semiconductor region and said 2nd semiconductor region being the same conductivity type.

[Claim 17] A manufacture method of semiconductor integrated circuit equipment characterized by including the following processes;

a conductor formed in the upper part of said 2nd silicon oxide film after forming the 2nd silicon oxide film on (a) semiconductor substrate characterized by providing the following -- by carrying out patterning of the film After forming the 2nd silicon nitride film on a process which forms a gate electrode of MISFET, and said semiconductor substrate including the upper part of the (b) aforementioned gate electrode, By etching a process which forms the 4th silicon oxide film in the upper part of said 2nd silicon nitride film, the 4th silicon oxide film of (c) above, and said 2nd silicon nitride film It is the 1st field of the lower part of said gate electrode by etching a process and the 2nd silicon oxide film of (d) above on which the upper part and a side attachment wall of said gate electrode of said MISFET are exposed isotropic. Expose an underside and said semiconductor substrate of said gate electrode, and it sets to the 2nd field of the lower part of said gate electrode. By heat-treating a process and the (e) aforementioned semiconductor substrate which leave said 2nd silicon oxide film Said 1st silicon oxide film formed in a front face of said semiconductor substrate in said 1st field in a process and the 1st field of (f) above which form the 1st silicon oxide film in a front face of said semiconductor substrate, and an underside of said gate electrode A crevice between said 1st silicon oxide films formed in an underside of said gate electrode

[Claim 18] Are the manufacture method of semiconductor integrated circuit equipment according to claim 17, and an impurity is introduced into an edge by the side of said 1st field of said gate electrode in self align. An impurity is introduced into an edge by the side of a process which forms the 1st semiconductor region in said semiconductor substrate, and said 2nd field of said gate electrode in self align. A manufacture method of semiconductor integrated

circuit equipment characterized by making high impurity concentration of said 1st semiconductor region lower than high impurity concentration of said 2nd semiconductor region including a process which forms the 2nd semiconductor region in said semiconductor substrate.

[Claim 19] The gate electrode of MISFET which it is the manufacture method of semiconductor integrated circuit equipment according to claim 17 or 18, and said MISFET constitutes nonvolatile memory, and constitutes a circumference circuit, and the gate electrode of MISFET which constitutes said nonvolatile memory are the manufacture method of the semiconductor integrated circuit equipment characterized by to be formed at a process which carries out patterning of the same electric-conduction film, and to form a gate insulator layer of MISFET which constitutes said circumference circuit at a process which forms said 2nd silicon oxide film.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention is applied to the semiconductor integrated circuit equipment which has the nonvolatile memory of the single MISFET structure which made the insulator layer trap the are recording field of a charge about semiconductor integrated circuit equipment and its manufacturing technology, and relates to effective technology.
[0002]
[Description of the Prior Art] The basic cellular structure of the nonvolatile memory formed on a silicon substrate The so-called floating-gate mold which is formed between gate oxide and the control gate (word line) of the upper part, and makes the floating (floating) gate insulated by the perimeter and the electric target the are recording field of a charge, Do not have such the floating gate but a gate insulator layer consists of cascade screens of a silicon oxide film and a silicon nitride film. It is divided roughly into the MNOS (Metal-gate Nitride Oxide Silicon) mold which makes the electron by which the trap was carried out into the above-mentioned silicon nitride film the are recording field of a charge.
[0003] Drawing 52 is the cross section showing the typical cellular structure of a floating-gate mold memory cell. this -- a memory cell -- a silicon substrate -- 101 -- a principal plane -- a top -- forming -- having had -- thickness -- ten -- nm -- about -- gate oxide -- 102 -- the upper part -- the floating gate -- 103 -- an interlayer insulation film -- 104 -- and -- control -- the gate -- (-- CG --) -- 105 -- sequential -- formation -- carrying out -- the floating gate -- 103 -- both sides -- a silicon substrate -- 101 -- the source -- (-- S --) -- 106 -- and -- a drain -- (-- D --) -- 107 -- having formed -- structure -- becoming -- **** .
[0004] the condition that there is no are recording of the threshold voltage (Vth) of the transistor which the writing of a memory cell poured in the electron 108 all over the floating gate 103, and was seen from the control gate 105 of an electron 108 -- comparing -- 3V-5 -- it carries out by making it go up about by V. Moreover, impregnation of the electron 108 to the floating gate 103 has the method in use drawn in the floating gate 103 with the positive voltage which impressed the about 107-drain hot electron generated by avalanche breakdown to the control gate 105.
[0005] On the other hand, drawing 53 is the cross section showing the typical cellular structure of an MNOS mold memory cell. Sequential formation of the gate electrode (PEG) 115a a silicon nitride film 113 and for writing/elimination is carried out in the upper part of the direct tunnel oxide film 112 of about 2nm of thickness with which this memory cell was formed on the principal plane of a silicon substrate 111. MISFET by which the source (S) 116 and the connection diffusion layer (drain) 117 were formed in the silicon substrate 111 of the both sides of gate electrode 115a (storage element section), It consists of MISFET(s) for selection by which gate electrode (SG)115b for selection was formed in the upper part of gate oxide 118, and the connection diffusion layer (source) 117 and the drain (D) 119 were formed in the silicon substrate 111 of the both sides of gate electrode 115b.
[0006] By controlling the potential of gate electrode 115a a silicon substrate 111 and for writing/elimination, pouring in an electron 108 completely and carrying out a trap into a silicon nitride film 113, from a silicon substrate 111 side through the direct tunnel oxide film 112, the writing of a memory cell raises the threshold voltage of MISFET of the storage element section, and performs it. Moreover, by controlling the potential of a silicon substrate 111 and gate electrode 115a, and emitting similarly, the electron which carried out the trap into the silicon nitride film 113 to a silicon substrate 111 side, the threshold voltage of MISFET of the storage element section is dropped, and elimination is also performed. In the case of this elimination actuation, since the threshold voltage of the storage element section is reduced to less than [0V], i.e., a depression field, in order to read, MISFET for selection described above in addition to MISFET of the storage element section is needed.

[0007] The electron by which the trap was carried out is independently contributed to the modulation of threshold voltage, respectively from the above-mentioned MNOS mold memory cell being a method of operation which carries out the trap of the electron into an insulator layer (silicon nitride film 113). Therefore, the fluctuation of the threshold voltage covering the channel whole region of the storage element section by partial leakage of the electron in the silicon nitride film 113 resulting from the defect in the direct tunnel film 112 is dramatically small. In other words, the retention property is excellent and it can be said that it is a memory cell method with high reliability.
[0008] Drawing 54 is the cross section showing the cellular structure which was indicated by United States Patent (USP) No. 5408115, and was named "Self-Aligned Split-Gate EEPROM Device." This memory cell carries out the laminating of gate oxide 122 and the gate electrode 123 for selection (SG) on the principal plane of a silicon substrate 121, and has structure which formed the sidewall gate electrode (SWG) 127 through the insulator layer of three layers which becomes the side-attachment-wall section of them from the silicon oxide film 124, a silicon nitride film 125, and the silicon oxide film 126. Moreover, the source (S) 128 is formed of the ion implantation which uses this sidewall gate electrode (SWG) 127 as a mask, and the drain (D) 129 is formed of the ion implantation which uses said gate electrode 123 for selection as a mask.
[0009] The writing of a memory cell is "1997 Symposium on VLSI Technology Digest ofTechnical Papers p63-p64". A drain 129 is made into touch-down potential, and it carries out by impressing the voltage of 5V, 9V, and 1V to the source 128, the sidewall gate electrode 127, and the selector-gate electrode 123, respectively as indicated.
[0010] Drawing 55 shows the potential distribution and field strength distribution of a channel field at the time of write-in actuation of the above-mentioned memory cell. In the voltage (5V) impressed between (Source S)-drains (D), the field strength which met in the direction of a channel like a graphic display since the most was impressed to the depletion layer of the source (S) serves as maximum in directly under [of a sidewall gate electrode (SWG)]. Therefore, it is accelerated in the high electric-field field near the source (S), and the electron which has run from the drain (D) to the channel field causes avalanche breakdown, into a silicon nitride film (125), it is poured in and the trap of the hot electron generated at this time is carried out by the high electric field of the lengthwise direction by the sidewall gate electrode (SWG). That is, the threshold voltage seen from the sidewall gate electrode (SWG) rises by carrying out the trap of the electron to the silicon nitride film [directly under] (125) of a sidewall gate electrode (SWG). The write-in method by this hot electron is the same on the method and basic target which draw the hot electron near [in the floating-gate mold memory cell mentioned above] the drain in the floating gate.
[0011] Moreover, read-out of the above-mentioned memory cell makes the source (128) touch-down potential, impresses the voltage of 1.8V to a sidewall gate electrode (127) and the gate electrode (123) for selection, and judges the modulation of the threshold voltage seen from the sidewall gate electrode (127) by the existence of the electron trap in a silicon nitride film (125) from drain current. In order that this memory cell may write in using a hot electron, even if it forms by thickness (for example, about 10nm) thicker than the direct tunnel oxide film of the MNOS mold memory cell which mentioned above the silicon oxide film [directly under] (124) of the silicon nitride film (125) to which the trap of the electron is carried out, drawing speed does not deteriorate. Moreover, defect density decreases, so that this silicon oxide film (124) is made into thick thickness, and the retention property of a memory cell improves as a result.
[0012] IEEE Electron Device Lett., and (vol.EDL-8, no.3, pp.93-95, March 1987) are indicating the nonvolatile memory of single MISFET structure without the control gate. The memory cell of this nonvolatile memory consists of a gate electrode of the polycrystalline silicon formed in the upper part of a gate insulator layer, and the source and the drain which were formed in the semiconductor substrate of the both sides of this gate electrode, and the gate insulator layer consists of three-tiered structures which sandwiched the silicon nitride film between two-layer silicon oxide films.
[0013] The writing of a memory cell performs the carrier near the drain impregnation and by carrying out a trap into a silicon nitride film. This memory cell is excellent in the retention property compared with the MNOS mold memory cell, in order that the carrier in the silicon nitride film inserted into the two-layer silicon oxide film may carry out localization to the narrow field near the drain.
[0014] JP,6-232416,A is indicating the nonvolatile memory of the single MISFET structure where the gate insulator layer and the trap film holding a carrier were stood in a row and formed in the upper part of the channel field between the source and a drain, and the gate electrode was formed in the upper part of this gate insulator layer and a trap film. A gate insulator layer consists of silicon oxide films, and the trap film consists of three-tiered structures which sandwiched the silicon nitride film between two-layer silicon oxide films.
[0015] The writing of a memory cell performs an electron silicon nitride film impregnation and by carrying out a trap through the lower layer silicon oxide film (tunnel oxide film) which constitutes some trap films. Since this memory cell forms the gate insulator layer of the usual enhancement MISFET, and the trap film of the memory section holding a carrier in the lower part of a single gate electrode, it can reduce cel area.

[0016]
[Problem(s) to be Solved by the Invention] Since the floating-gate mold memory cell mentioned above carries out the laminating of the control gate (word line) to the upper part of the floating gate, it can design cel area comparatively small and has the cellular structure suitable for large capacity-ization. on the other hand, although it can say that the MNOS mold memory cell be excellent in the retention property compared with the floating gate mold memory cell, and be a cell method with high reliability, since two basic elements be need for the storage element section and selection, the cel area in the same layout rule become large [a floating gate mold memory cell] about 4 to 5 times, and large capacity-ization have the defect of not be suitable.
[0017] Moreover, the memory cell indicated by United States Patent (USP) No. 5408115 has the scalability and the MNOS mold memory cell which are equal to a floating-gate mold memory cell, and the high reliability more than an EQC. However, compared with a floating-gate mold memory cell, writing/elimination actuation becomes complicated and the area of the circumference circuit needed as a result increases the cellular structure which has a gate electrode for selection, and a sidewall gate electrode. And for a certain reason, the width of face of a sidewall gate electrode increased by about 100nm by 5 to 7 times the gate resistance usual in the wiring resistance, this read, and deterioration of speed is caused. Furthermore, although the width of face of between the gate electrode for selection and sidewall gate electrodes (i.e., the channel field [directly under] of the field where the laminating of a silicon oxide film (124), a silicon nitride film (125), and the silicon oxide film (126) was carried out to the longitudinal direction) is as slight as about 30nm, the gate electrode does not exist in the upper part. Therefore, this field acts as parasitism resistance, reduces the drain current at the time of read-out, and reads, and there is a problem of degrading speed.
[0018] The object of this invention is to offer the nonvolatile memory equipped with the new cellular structure having the scalability and the MNOS mold memory cell which are equal to a floating-gate mold memory cell, and the high reliability more than an EQC, and its manufacture method.
[0019] The other objects and the new feature will become clear from description and the accompanying drawing of this description along [said] this invention.
[0020]
[Means for Solving the Problem] It will be as follows if an outline of a typical thing is briefly explained among invention indicated in this application.
[0021] A gate electrode connected to a word line and an electric target is formed on a gate insulator layer by which nonvolatile memory of the invention in this application was formed on a semiconductor substrate of the 1st conductivity type. The 1st and 2nd semiconductor region of the 2nd conductivity type which constitutes the source and a drain is formed in said semiconductor substrate. A memory cell of a non-volatile is constituted by MISFET by which a channel field is formed between said 1st semiconductor region and said 2nd semiconductor region. Said gate insulator layer Said 1st semiconductor region side consists of an insulator layer of three layers which carried out the laminating of the 1st silicon oxide film, a silicon nitride film, and the 2nd silicon oxide film at least.
[0022] Writing of said memory cell makes high potential said 2nd semiconductor region of a selected memory cell rather than said 1st semiconductor region, and is performed by injecting into an electron trap in a silicon nitride film a hot electron generated in the 2nd conductivity-type semiconductor region of low high impurity concentration.
[0023] In addition, it will be as follows, if the term division of the outline of invention indicated by this application is carried out and it is explained.
[0024] 1. Gate Electrode Connected to Word Line and Electric Target is Formed on Gate Insulator Layer Formed on Semiconductor Substrate of 1st Conductivity Type. The 1st and 2nd semiconductor region of the 2nd conductivity type which constitutes the source and a drain is formed in said semiconductor substrate. It is semiconductor integrated circuit equipment with which a memory cell of a non-volatile was constituted by MISFET by which a channel field is formed between said 1st semiconductor region and said 2nd semiconductor region. Said 1st semiconductor region side at least said gate insulator layer The 1st silicon oxide film, It is semiconductor integrated circuit equipment characterized by consisting of an insulator layer of three layers which carried out the laminating of a silicon nitride film and the 2nd silicon oxide film, and carrying out by writing of said memory cell making said 2nd semiconductor region high potential rather than said 1st semiconductor region.
[0025] 2. Gate Electrode Connected to Word Line and Electric Target is Formed on Gate Insulator Layer Formed on Semiconductor Substrate. The 1st and 2nd semiconductor region of the 2nd conductivity type which constitutes the source and a drain is formed in said semiconductor substrate. It is semiconductor integrated circuit equipment with which a memory cell of a non-volatile was constituted by MISFET by which a channel field is formed between said 1st semiconductor region and said 2nd semiconductor region. Said 1st semiconductor region side at least said gate insulator layer The 1st silicon oxide film, High impurity concentration of a portion which consists of an insulator layer of three

layers which carried out the laminating of a silicon nitride film and the 2nd silicon oxide film, and extends in the lower part of said gate electrode of said 1st semiconductor region Semiconductor integrated circuit equipment characterized by pouring said hot electron into said silicon nitride film by being lower than high impurity concentration of a portion which extends in the lower part of said gate electrode of said 2nd semiconductor region, and generating a hot electron in said 1st semiconductor region side.

[0026] 3. Gate Electrode Connected to Word Line and Electric Target is Formed on Gate Insulator Layer Formed on Semiconductor Substrate. The 1st and 2nd semiconductor region of the 2nd conductivity type which constitutes the source and a drain is formed in said semiconductor substrate. It is semiconductor integrated circuit equipment with which a memory cell of a non-volatile was constituted by MISFET by which a channel field is formed between said 1st semiconductor region and said 2nd semiconductor region. Said 1st semiconductor region side said gate insulator layer The 1st silicon oxide film, It consists of an insulator layer of three layers which carried out the laminating of a silicon nitride film and the 2nd silicon oxide film. High impurity concentration of a portion to which said 2nd semiconductor region side extends in the lower part of said gate electrode of said 1st semiconductor region by consisting of a silicon oxide film is semiconductor integrated circuit equipment characterized by differing from high impurity concentration of a portion which extends in the lower part of said gate electrode of said 2nd semiconductor region.

[0027] 4. High impurity concentration of a portion which extends in the lower part of said gate electrode of said 1st semiconductor region in said claims 1 or 3 is semiconductor integrated circuit equipment characterized by being lower than high impurity concentration of a portion which extends in the lower part of said gate electrode of said 2nd semiconductor region.

[0028] 5. It is semiconductor integrated circuit equipment characterized by consisting of an insulator layer of three layers to which, as for said gate insulator layer, said 1st semiconductor region side carried out the laminating of said 1st silicon oxide film, a silicon nitride film, and the 2nd silicon oxide film in said claims 1, 2, or 4, and said 2nd semiconductor region side consisting of a silicon oxide film.

[0029] 6. It is semiconductor integrated circuit equipment characterized by said gate insulator layer having the electric capacity thickness with almost same said 1st semiconductor region side and said 2nd semiconductor region side in any 1 term of said claims 1-5.

[0030] 7. It is semiconductor integrated circuit equipment characterized by consisting of an insulator layer of three layers to which, as for said gate insulator layer, said said 1st semiconductor region and 2nd semiconductor region side carried out the laminating of said 1st silicon oxide film, a silicon nitride film, and the 2nd silicon oxide film in said claims 1, 2, 4, 5, or 6.

[0031] 8. It is semiconductor integrated circuit equipment characterized by carrying out by pouring in a hot electron into said silicon nitride film with which writing of said memory cell constitutes said a part of gate insulator layer in said claims 1, 3, 4, 5, 6, or 7.

[0032] 9. Thickness of said 1st silicon oxide film formed in a lower layer of said silicon nitride film in any 1 term of said claims 1-8 among said insulator layers of three layers which constitute said a part of gate insulator layer [at least] is semiconductor integrated circuit equipment characterized by being thicker than thickness to which direct tunnel current flows.

[0033] 10. It is semiconductor integrated circuit equipment which said 2nd semiconductor region consists of a semiconductor region of the 1st conductivity type with which the end extends in the lower part of said gate electrode, and a semiconductor region of the 2nd conductivity type which the end estranged from said gate electrode in any 1 term of said claims 1-9, and is characterized by said 1st semiconductor region consisting of the 2nd conductivity type.

[0034] 11. It is semiconductor integrated circuit equipment characterized by carrying out by read-out of said memory cell making said 1st semiconductor region high potential rather than said 2nd semiconductor region in any 1 term of said claims 1-10.

[0035] 12. It is semiconductor integrated circuit equipment characterized by carrying out by read-out of said memory cell making said 2nd semiconductor region high potential rather than said 1st semiconductor region in any 1 term of said claims 1-10.

[0036] 13. Source Line is Formed of Plug Embedded in Any 1 Term of Said Claims 1-12 at 1st Connection Hole Formed in Insulator Layer of One Upper Part of Said 1st and 2nd Semiconductor Region. Semiconductor integrated circuit equipment characterized by connecting a bit line to another side of said 1st and 2nd semiconductor region through a plug embedded at the 2nd connection hole formed in said insulator layer of the upper part of another side of said 1st and 2nd semiconductor region.

[0037] 14. It is semiconductor integrated circuit equipment characterized by forming said 1st connection hole and said 2nd connection hole by self align to a space of a gate electrode of said MISFET in said claim 13.

[0038] 15. It is semiconductor integrated circuit equipment characterized by consisting of said MISFET from which said memory cell constitutes the storage element section in any 1 term of claims 1-14, and MISFET for selection.
[0039] 16. It is semiconductor integrated circuit equipment characterized by said 1st semiconductor region and said 2nd semiconductor region being the same conductivity type in claims 1-9 and any 1 term of 11-15.
[0040] 17. A Manufacture Method of Semiconductor Integrated Circuit Equipment Characterized by Including the Following Processes;
(a) a process which forms a silicon nitride film in the upper part of said 1st silicon oxide film after forming the 1st silicon oxide film on a semiconductor substrate, and (b) -- by carrying out patterning of said 1st silicon oxide film and said silicon nitride film It leaves said 1st silicon oxide film and said silicon nitride film to the 1st field on said semiconductor substrate. A process which removes said 1st silicon oxide film and said silicon nitride film of the 2nd field, (c) A process which forms the 2nd silicon oxide film in the upper part of said silicon nitride film of said 1st field on said semiconductor substrate, and said 2nd field on said semiconductor substrate, (d) -- a conductor formed in the upper part of said 2nd silicon oxide film -- a process which forms a gate electrode of MISFET by carrying out patterning of the film on said 2nd silicon oxide film of said 1st and 2nd field.
[0041] 18. A Manufacture Method of Semiconductor Integrated Circuit Equipment Characterized by Including the Following Processes;
(a) a conductor formed in the upper part of said 2nd silicon oxide film after forming the 2nd silicon oxide film on a semiconductor substrate -- by carrying out patterning of the film After forming the 2nd silicon nitride film on a process which forms a gate electrode of MISFET, and said semiconductor substrate including the upper part of the (b) aforementioned gate electrode, By etching a process which forms the 4th silicon oxide film in the upper part of said 2nd silicon nitride film, the 4th silicon oxide film of (c) above, and said 2nd silicon nitride film By etching a process and the 2nd silicon oxide film of (d) above on which the upper part and a side attachment wall of said gate electrode of said MISFET are exposed isotropic In the 1st field of the lower part of said gate electrode, expose an underside and said semiconductor substrate of said gate electrode, and it sets to the 2nd field of the lower part of said gate electrode. By heat-treating a process and the (e) aforementioned semiconductor substrate which leave said 2nd silicon oxide film In a process and the 1st field of (f) above which form the 1st silicon oxide film in a front face of said semiconductor substrate, and an underside of said gate electrode in said 1st field A process which forms the 2nd silicon nitride film on said semiconductor substrate including a crevice between said 1st silicon oxide film formed in a front face of said semiconductor substrate, and said 1st silicon oxide film formed in an underside of said gate electrode.
[0042] 19. Introduce Impurity into Edge by the side of Said 1st Field of Said Gate Electrode in Self Align in Claims 17 or 18. An impurity is introduced into an edge by the side of a process which forms the 1st semiconductor region in said semiconductor substrate, and said 2nd field of said gate electrode in self align. A manufacture method of semiconductor integrated circuit equipment characterized by making high impurity concentration of said 1st semiconductor region lower than high impurity concentration of said 2nd semiconductor region including a process which forms the 2nd semiconductor region in said semiconductor substrate.
[0043] 20. A gate electrode of MISFET which said MISFET constitutes nonvolatile memory and constitutes a circumference circuit in claims 17, 18, or 19, and a gate electrode of MISFET which constitutes said nonvolatile memory are the manufacture method of semiconductor integrated circuit equipment characterized by to be formed at a process which carries out patterning of the same electric conduction film, and to form a gate insulator layer of MISFET which constitutes said circumference circuit at a process which forms said 2nd silicon oxide film.
[0044]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to details based on a drawing. In addition, in the complete diagram for explaining the gestalt of operation, the same sign is given to the member which has the same function, and explanation of the repeat is omitted.
[0045] (Gestalt 1 of operation) Drawing 1 is the outline circuit diagram showing the body of the flash memory (package elimination mold nonvolatile memory) which is the gestalt of 1 operation of this invention.
[0046] In the memory cell array (MA) of this flash memory Two or more word lines WL (WL1 -WLm) and two or more source lines SL (SL1 -SLm/2) which extend in the longitudinal direction (the direction of X) of drawing Two or more memory cells M (M11-Mnm) which consisted of two or more bit line DL (DL1 -DLn) and the MISFET structures mentioned later which extend in the direction of Y which intersects perpendicularly with these are formed.
[0047] Each of the above-mentioned word line WL (WL1 -WLm) is connected to the gate electrode of two or more memory cells M arranged along the direction of X, and the end section is connected to the low decoder (X-DEC). One each of the source line SL (SL1 -SLm/2) is arranged between [each] two word lines WL, and is connected to the source with which two memory cells M which adjoin in the direction of Y are common. Moreover, the end section of

these source lines SL (SL1 -SLm/2) is connected to the common source line CSL arranged at the periphery of a memory cell array (MA). Each of bit line DL (DL1 -DLn) is connected to the drain with which two memory cells M which adjoin in the direction of Y are common, and the end section is connected to the column decoder (Y-DEC) and the sense amplifier (SA).

[0048] The plan in which the important section cross section of the semiconductor substrate in which the one section each of the circumference circuit where drawing 2 adjoins the above-mentioned memory cell array and it is shown, and drawing 3 (A) show the conductor-layer pattern for about four memory cells, and drawing 3 (B) are the plans showing the conductor-layer pattern for about 12 memory cells.

[0049] The well 5 is formed in the memory cell array field of the semiconductor substrate 1 which consists of single crystal silicon of p mold p mold, and the well 6 is formed in the circumference circuit field n mold with the well 5 p mold. moreover, p mold of a memory cell array field -- the lower part of a well 5 -- this p mold -- deep n mold for separating a well 5 electrically from other fields of the semiconductor substrate 1 -- the well 4 is formed. p mold -- a well 5 and n mold -- the field oxide 2 for isolation which consisted of silicon oxide films is formed in each front face of a well 6.

[0050] MISFETQm of the n channel mold of a memory cell array field which constitutes a memory cell in a well 5 is formed p mold. Moreover, p mold, the n channel mold MISFETQn of a circumference circuit field which constitutes a part of circumference circuit in a well 5 is formed, and the p channel mold MISFETQp which constitutes a part of other circumference circuits is formed in the well 6 n molds.

[0051] Gate electrode 10a by which MISFETQm which constitutes a memory cell was formed mainly on the gate insulator layer, n+ in which an end extends to the lower part of gate electrode 10a Mold semiconductor region 13 (drain), n+ formed so that it might offset to gate electrode 10a Mold semiconductor region 15 (high concentration source), n+ n in which it is formed in the perimeter of the mold semiconductor region 15, and an end extends to the lower part of gate electrode 10a - It consists of a mold semiconductor region 11 (low concentration source) and a channel formation field (p mold well 5) inserted into these sources and a drain. Gate electrode 10a is constituted by a word line WL and one, and the source (n+ the mold semiconductor region 15, n - mold semiconductor region 11) is constituted by the source line SL and one.

[0052] It consists of polycide films which carried out the laminating of the W (tungsten) silicide film to the upper part of the polycrystalline silicon film of n mold, and, as for gate electrode 10a, the sidewall spacer 16 which consisted of silicon oxide films is formed in the side attachment wall. Moreover, a drain side consists of silicon oxide films 9 of one layer, and the gate insulator layer formed in the lower part of gate electrode 10a consists of insulator layers of three layers to which the source side carried out the laminating of the silicon oxide film 7 and the silicon nitride film 8 to the lower layer of the silicon oxide film 9.

[0053] The p channel mold MISFETQp of a circumference circuit Gate electrode 10b formed mainly on the gate insulator layer (silicon oxide film 9), p+ of the couple formed so that it might offset to gate electrode 10b Mold semiconductor region 14 (the source, drain), p of the couple in which an end extends to the lower part of gate electrode 10b - It consists of a mold semiconductor region 12 and a channel formation field (p mold well 5) inserted into these sources and a drain. Moreover, the n channel mold MISFETQn of a circumference circuit Gate electrode 10c formed mainly on the gate insulator layer (silicon oxide film 9), n+ of the couple formed so that it might offset to gate electrode 10c Mold semiconductor region 15 (the source, drain), n of the couple in which an end extends to the lower part of gate electrode 10c - It consists of a mold semiconductor region 11 and a channel formation field (p mold well 5) inserted into these sources and a drain. That is, the p channel mold MISFETQp of a circumference circuit and the n channel mold MISFETQn are LDD (Lightly Doped Drain). It consists of structures. Gate electrode 10b of the p channel mold MISFETQp and gate electrode 10c of the n channel mold MISFETQn consist of polycide films as well as gate electrode 10a of a memory cell, and the sidewall spacer 16 which consisted of silicon oxide films is formed in those side attachment walls.

[0054] The silicon oxide film 17 of thick thickness is formed in the upper part of the above-mentioned memory cell (MISFETQm), the p channel mold MISFETQp, and the n channel mold MISFETQn, and the wiring 23-27 which consisted of aluminum alloy films is further formed in the upper part.

[0055] The wiring 23 formed in the memory cell array field constitutes bit line DL, and is connected with the drain (n+ mold semiconductor region 13) of a memory cell through the contact hole 20 formed in the silicon oxide film 17. Moreover, the wiring 24 and 25 among the wiring 24-27 formed in the circumference circuit field the contact hole 21 of the couple formed in the silicon oxide film 17 -- leading -- p+ mold semiconductor region 14 (the source --) of the couple of the p channel mold MISFETQp Wiring 26 and 27 leads the contact hole 22 of the couple formed in the silicon oxide film 17 by connecting with a drain, and it is n+ of the couple of the n channel mold MISFETQn. It connects with

the mold semiconductor region 15 (the source, drain).
[0056] Next, program actuation of the above-mentioned flash memory is explained using drawing 4 (outline cross section showing about one memory cell), drawing 5 (operating voltage table of a memory cell), and drawing 6 (graph which shows the potential distribution and field strength distribution of a channel field at the time of write-in actuation of a memory cell).
[0057] Write-in actuation makes the source (11 15) of the selected memory cell (MISFETQm) touch-down potential (0V), and impresses the positive voltage of 5V to a gate electrode (10a) and a drain (13), respectively. The peak of field strength as shown in the edge of the low concentration source (11) at drawing 6 arises by this, the hot electron (e-) generated in this field (low concentration source side) is injected into the electron trap in a silicon nitride film 8, and writing is performed when the threshold voltage seen from the gate electrode (10a) rises.
[0058] Moreover, read-out actuation makes the source (11 15) of the selected memory cell similarly touch-down potential (0V), impresses the positive voltage of 2V to a gate electrode (10a) and a drain (13), respectively, and is performed. Elimination actuation is performed by dropping the threshold voltage seen from the gate electrode (10a) by making the drain (13) of a memory cell into touch-down potential (0V), impressing the positive voltage of 5V to the source (11 15), impressing the negative voltage of -10V to a gate electrode (10a), respectively, and emitting the electron by which the trap was carried out into the silicon nitride film 8 to a substrate (p mold well 5) side.
[0059] Next, an example of the manufacture method of the above-mentioned nonvolatile memory is explained using drawing 7 - drawing 18 (important section cross section of the semiconductor substrate in which the one section each of the circumference circuit field which adjoins a memory cell array field and it is shown).
[0060] first, the semiconductor substrate 1 which consists of single crystal silicon of p mold which has about [10ohmcm] specific resistance as shown in drawing 7 -- preparing -- the front face -- selective oxidation (LOCOS) -- after forming field oxide 2 of about 500nm of thickness by law, the silicon oxide film 3 of about 20nm of thickness is formed in the front face of the element formation field surrounded by the above-mentioned field oxide 2 by oxidizing the semiconductor substrate 1 thermally. The silicon oxide film 3 is used as a mask at the time of carrying out the ion implantation of the impurity to the semiconductor substrate 1 at the following process.
[0061] next, it is shown in drawing 8 -- as -- n mold deep to the semiconductor substrate 1 of a memory cell array field -- p mold shallow to some (n channel mold MISFET formation field) semiconductor substrates 1 of a memory cell array field and a circumference circuit after forming a well 4 -- a well 5 -- forming -- n mold shallow to some [other] (p channel mold MISFET formation field) semiconductor substrates 1 of a circumference circuit -- a well 6 is formed.
[0062] The deep photoresist film of about 5 micrometers of thickness by which the well 4 prepared the aperture in the memory cell array field n mold is used as a mask, and on condition that acceleration energy 3000keV and 1x1013/cm2 of doses, the ion implantation of the n mold impurity (Lynn) is carried out at the semiconductor substrate 1, and it forms. Moreover, the shallow photoresist film of about 2.5 micrometers of thickness by which the well 5 prepared the aperture in the memory cell array field and the n channel mold MISFET formation field p mold is used as a mask, and on condition that acceleration energy 450keV, 1x1013/cm2 of doses and acceleration energy 200keV, and 3x1012/cm2 of doses, the ion implantation of the p mold impurity (boron) is carried out at the semiconductor substrate 1, and it forms. Furthermore, the shallow photoresist film of about 2.5 micrometers of thickness by which the well 6 prepared the aperture in the p channel mold MISFET formation field n mold is used as a mask, and on condition that acceleration energy 1000keV, dose 1.5x1013-/cm2, acceleration energy 370keV, 3x1013/cm2 of doses and acceleration energy 180keV, and 1x1012/cm2 of doses, the ion implantation of the n mold impurity (Lynn) is carried out at the semiconductor substrate 1, and it forms.
[0063] In addition, the ion implantation of the impurity (boron) for adjusting a memory cell (MISFETQm) and the threshold voltage (Vth) of the n channel mold MISFETQn is simultaneously carried out at the ion implantation process for [above-mentioned] forming a well 5 p mold (acceleration energy 50keV, dose 1.2x1012-/cm2). Moreover, the ion implantation of the impurity (boron) for adjusting the threshold voltage (Vth) of the p channel mold MISFETQp is simultaneously carried out at the ion implantation process for forming a well 6 n molds (acceleration energy 20keV, dose 1.5x1012-/cm2).
[0064] Next, p molds, a well 5 and after removing the silicon oxide film 3 of each front face of a well 6 by wet etching n molds, as shown in drawing 9 the semiconductor substrate 1 -- about 750 degrees C -- oxidizing thermally -- p mold -- a well 5 and n mold -- the silicon oxide film 7 of about 7nm of thickness is formed in each front face of a well 6, and the silicon nitride film 8 of about 7nm of thickness is further deposited on the upper part of the silicon oxide film 7 with an about 800-degree C heat CVD method.
[0065] Next, as shown in drawing 10 , patterning of the above-mentioned silicon nitride film 8 and the silicon oxide film 7 is carried out, and it leaves these films only a source formation field and near the memory cell. Patterning of a

silicon nitride film 8 is performed by the dry etching which used as the mask the photoresist film of about 1 micrometer of thickness which prepared the aperture in the above-mentioned source formation field and its near, and after patterning of the silicon oxide film 7 removes the above-mentioned photoresist film by ashing, it is performed by the dry etching which used the silicon nitride film 8 as the mask. The above-mentioned two-layer insulator layer (the silicon oxide film 7, silicon nitride film 8) which it leaves to a source formation field and its near adjusts the width of face so that the length (gate length lay length) of the portion located in the lower part of gate electrode 10a formed at a next process may be set to 20nm - about 200nm.

[0066] next, it is shown in drawing 11 -- as -- the semiconductor substrate 1 -- about 800 degrees C -- oxidizing thermally -- p mold -- a well 5 and n mold -- the silicon oxide film 9 of about 15nm of thickness is formed in each front face of a well 6. Since the silicon nitride film 8 of a memory cell array field also oxidizes simultaneously at this time, the silicon oxide film 9 of about 2nm of thickness is formed also in that front face.

[0067] Next, as shown in drawing 12 , gate electrode 10a of a memory cell (MISFETQm) is formed on the silicon oxide film 9 of a memory cell array field, and gate electrode 10b of the p channel mold MISFETQn and gate electrode 10c of the n channel mold MISFETQp are formed on the silicon oxide film 9 of a circumference circuit field. After the gate electrodes 10a, 10b, and 10c deposit about 100nm of thickness, the polycrystalline silicon film of 2x1020/of about three Lynn concentration cm, and W silicide film of about 50nm of thickness with an about 600-degree C heat CVD method on the silicon oxide film 9, by the dry etching which used the photoresist film as the mask, they carry out patterning of these films, and form them.

[0068] next, the thing done for the ion implantation of the n mold impurity (Lynn) all over the semiconductor substrate 1 on condition that acceleration energy 40keV and 1x1013/cm2 of doses as shown in drawing 13 -- p mold of each both sides of the gate electrodes 10a and 10c -- n mold of the both sides of a well 5 and gate electrode 10b -- a well 6 -- n- of low high impurity concentration The mold semiconductor region 11 is formed.

[0069] Next, n+ which constitutes the drain of a memory cell by using as a mask the photoresist film of about 1 micrometer of thickness which prepared the aperture in the drain formation field of a memory cell, and carrying out the ion implantation of the n mold impurity (arsenic) to a well 5 p mold on condition that acceleration energy 50keV and 3x1015/cm2 of doses as shown in drawing 14 The mold semiconductor region 13 is formed.

[0070] Next, as shown in drawing 15 , the photoresist film of about 1 micrometer of thickness which prepared the aperture in the p channel mold MISFET formation field is used as a mask. By carrying out the ion implantation of the p mold impurity (2 boron fluoride) to a well 6 n mold on condition that acceleration energy 50keV and 2x1013/cm2 of doses n mold of the both sides of gate electrode 10b -- a well 6 -- said n- the mold semiconductor region 11 -- compensating -- p- of low high impurity concentration The mold semiconductor region 12 is formed.

[0071] Next, as shown in drawing 16 , after depositing the silicon oxide film (not shown) of about 200nm of thickness with a CVD method on the semiconductor substrate 1, the sidewall spacer 16 with a width of face of about 150nm is formed in each side attachment wall of the gate electrodes 10a, 10b, and 10c by carrying out anisotropic etching of this silicon oxide film. At this time, the silicon oxide film 9 and silicon nitride film 8 which have covered the source formation field of a memory cell are also etched simultaneously.

[0072] Next, p+ of the high high impurity concentration which constitutes the source of the p channel mold MISFET, and a drain by using as a mask the photoresist film of about 1 micrometer of thickness which prepared the aperture in the p channel mold MISFET formation field, and carrying out the ion implantation of the p mold impurity (2 boron fluoride) to a well 6 n mold on condition that acceleration energy 50keV and 3x1015/cm2 of doses as shown in drawing 17 The mold semiconductor region 14 is formed.

[0073] Then, the photoresist film of about 1 micrometer of thickness which prepared the aperture in the source formation field of a memory cell and the n channel mold MISFET formation field is used as a mask. By carrying out the ion implantation of the n mold impurity (arsenic) to a well 5 p mold on condition that acceleration energy 50keV and 2x1015/cm2 of doses n+ of the high high impurity concentration which constitutes the source of a memory cell The mold semiconductor region 15, the source of the n channel mold MISFET, and n+ of the high high impurity concentration which constitutes a drain The mold semiconductor region 15 is formed. At the process so far, a memory cell (MISFETQm) and MISFET (the n channel mold MISFETQn, the p channel mold MISFETQp) of a circumference circuit are completed.

[0074] Next, as shown in drawing 18 , after depositing the silicon oxide film 17 of about 500nm of thickness with a CVD method on the semiconductor substrate 1, contact holes 20, 21, and 22 are formed in the upper part of the drain of a memory cell, the source of the n channel mold MISFETQn, the upper part of a drain and the source of the p channel mold MISFETQp, and the upper part of a drain, respectively by using a photoresist film as a mask and carrying out dry etching of the silicon oxide film 17.

[0075] Then, aluminum alloy film of about 500nm of thickness is deposited by the sputtering method on the silicon oxide film 17 including the interior of contact holes 20-22, and the flash memory of the gestalt of this operation shown in said drawing 2 carries out abbreviation completion by carrying out patterning of this aluminum alloy film by the dry etching which used the photoresist film as the mask, and forming wiring 23-27.
[0076] Since the flash memory of the gestalt of this operation constituted as mentioned above consists of MISFET(s) with a single memory cell, it does not make the area of the circumference circuit which can perform writing/elimination actuation comparatively simple, and needs it increase like the conventional floating-gate mold memory cell. Moreover, a manufacturing process also becomes simple.
[0077] Since high resistance wiring like the memory cell equipped with the conventional sidewall gate electrode on the occasion of read-out actuation is not used for the flash memory of the gestalt of this operation, deterioration of read-out speed does not generate it. Moreover, in the case of write-in actuation, positive voltage is impressed to a gate electrode and a drain, since the method which injects into the electron trap in a silicon nitride film the hot electron generated near the source is adopted, when the source of touch-down potential and the gate inter-electrode potential difference become large, injection efficiency improves and low-battery actuation is attained more compared with the conventional cellular structure.
[0078] Since the gate electrode of a memory cell has covered the whole surface of a channel field, the flash memory of the gestalt of this operation does not have generating of the parasitism resistance in directly under [which poses a problem by the cellular structure equipped with the conventional sidewall gate electrode / sidewall gate electrode-control gate inter-electrode / insulator layer], and does not cause lowering of the drain current at the time of read-out actuation.
[0079] Since the manufacture method of the flash memory of the gestalt this operation forms the gate insulator layer by the side of the source of a memory cell (insulator layer of three layers which consists of the silicon oxide film 7, a silicon nitride film 8, and a silicon oxide film 9) by self align (self aryne) to a gate electrode, it can design in a cel area equivalent to the conventional floating-gate mold memory cell, and nonvolatile memory excellent in scalability can be realized.
[0080] (Gestalt 2 of operation) The manufacture method of the flash memory of the gestalt this operation is explained using drawing 19 - drawing 33 (important section cross section of the semiconductor substrate in which the one section each of the circumference circuit field which adjoins a memory cell array field and it is shown).
[0081] First, as shown in drawing 19 , after forming field oxide 2 in the front face of the semiconductor substrate 1 which consists of single crystal silicon of p mold, the silicon oxide film 3 is formed in the front face of the element formation field surrounded by field oxide 2. then, n mold deep to the semiconductor substrate 1 of a memory cell array field -- p mold shallow to some (n channel mold MISFET formation field) semiconductor substrates 1 of a memory cell array field and a circumference circuit after forming a well 4 -- a well 5 -- forming -- n mold shallow to some [other] (p channel mold MISFET formation field) semiconductor substrates 1 of a circumference circuit -- a well 6 is formed. The process so far is the same as the gestalt 1 of said operation.
[0082] Next, as the semiconductor substrate 1 is oxidized thermally at about 800 degrees C, and are shown in drawing 20 and it is shown in drawing 21 p mold after forming gate oxide 30 of about 15nm of thickness in each front face of a well 6 n molds, a well 5 and By using a photoresist film as a mask and carrying out dry etching of this polycrystalline silicon film 31, after depositing a polycrystalline silicon film (not shown) about 200 thickness with an about 600-degree C heat CVD method on the semiconductor substrate 1 The gate electrodes 31b and 31c of gate electrode 31a of a memory cell and a circumference circuit are formed.
[0083] Next, as shown in drawing 22 , after depositing the silicon nitride film 32 of about 20nm of thickness with a CVD method on the semiconductor substrate 1 including the upper part of the above-mentioned gate electrodes 31a, 31b, and 31c, the silicon oxide film 33 of about 50nm of thickness is deposited on the upper part of a silicon nitride film 32 with a CVD method.
[0084] Next, as shown in drawing 23 , after using as a mask the photoresist film of about 1 micrometer of thickness which prepared the aperture a source formation field and near the memory cell, carrying out wet etching of the silicon oxide film 33, and removing the above-mentioned photoresist film by ashing continuously, the silicon nitride film 32 which has covered the source formation field and gate electrode 31a of near of a memory cell is removed by using the silicon oxide film 33 as a mask, and carrying out wet etching of the silicon nitride film 32.
[0085] Next, as shown in drawing 24 , the gate oxide 30 which has covered the source formation field of a memory cell by the wet etching which used the above-mentioned silicon nitride film 32 as the mask is removed. At this time, the gate oxide 30 of the lower part of gate electrode 31a by which adjoined the source formation field and pattern formation was carried out is also etched, and that part is removed ranging from the edge to width of face of about 70nm (undercut).

[0086] next, p mold which oxidized the semiconductor substrate 1 thermally at about 750 degrees C, and was exposed a source formation field and near the memory cell as shown in drawing 25 -- the silicon oxide film 34 of about 5nm of thickness is formed in the front face of a well 5. At this time, gate electrode 31a exposed near the source formation field of a memory cell also oxidizes simultaneously, and the silicon oxide film 35 of about 5nm of thickness is formed in that front face.
[0087] Next, as shown in drawing 26 , the silicon nitride film 36 of about 10nm of thickness is deposited with a CVD method on the semiconductor substrate 1. Thereby, the gate insulator layer of three layers which is from the silicon oxide film 34, a silicon nitride film 36, and the silicon oxide film 35 on the source formation field side of the lower part of gate electrode 10a is formed.
[0088] next, the thing done for the ion implantation of the n mold impurity (Lynn) all over the semiconductor substrate 1 on condition that acceleration energy 40keV and 1x1013/cm2 of doses as shown in drawing 27 -- p mold of each both sides of the gate electrodes 10a and 10c -- n mold of the both sides of a well 5 and gate electrode 10b -- a well 6 -- n- of low high impurity concentration The mold semiconductor region 37 is formed.
[0089] Next, n+ which constitutes the drain of a memory cell by using as a mask the photoresist film of about 1 micrometer of thickness which prepared the aperture in the drain formation field of a memory cell, and carrying out the ion implantation of the n mold impurity (arsenic) to a well 5 p mold on condition that acceleration energy 50keV and 3x1015/cm2 of doses as shown in drawing 28 The mold semiconductor region 39 is formed.
[0090] Next, as shown in drawing 29 , the photoresist film of about 1 micrometer of thickness which prepared the aperture in the p channel mold MISFET formation field is used as a mask. By carrying out the ion implantation of the p mold impurity (2 boron fluoride) to a well 6 n mold on condition that acceleration energy 50keV and 2x1013/cm2 of doses n mold of the both sides of gate electrode 31b -- a well 6 -- said n- the mold semiconductor region 37 -- compensating -- p- of low high impurity concentration The mold semiconductor region 38 is formed.
[0091] Next, as shown in drawing 30 , after depositing the silicon nitride film of about 200nm of thickness with a CVD method on the semiconductor substrate 1, the sidewall spacer 42 with a width of face of about 150nm is formed in each side attachment wall of the gate electrodes 31a, 31b, and 31c by carrying out anisotropic etching of this silicon nitride film. At this time, the silicon oxide film 35 and silicon nitride film 35 which have covered the upper part of the gate electrodes 31a, 31b, and 31c are also etched simultaneously, and the front face of the gate electrodes 31a, 31b, and 31c exposes them.
[0092] Next, p+ of the high high impurity concentration which constitutes the source of the p channel mold MISFET, and a drain by using as a mask the photoresist film of about 1 micrometer of thickness which prepared the aperture in the p channel mold MISFET formation field, and carrying out the ion implantation of the p mold impurity (2 boron fluoride) to a well 6 n mold on condition that acceleration energy 50keV and 3x1015/cm2 of doses as shown in drawing 31 The mold semiconductor region 40 is formed.
[0093] Then, the photoresist film of about 1 micrometer of thickness which prepared the aperture in the source formation field of a memory cell and the n channel mold MISFET formation field is used as a mask. By carrying out the ion implantation of the n mold impurity (arsenic) to a well 5 p mold on condition that acceleration energy 50keV and 2x1015/cm2 of doses n+ of the high high impurity concentration which constitutes the source of a memory cell The mold semiconductor region 41, the source of the n channel mold MISFET, and n+ of the high high impurity concentration which constitutes a drain The mold semiconductor region 41 is formed. At the process so far, a memory cell (MISFETQm) and MISFET (the n channel mold MISFETQn, the p channel mold MISFETQp) of a circumference circuit are completed.
[0094] Next, after removing the silicon oxide film 34 which carried out wet etching of the front face of the semiconductor substrate 1, and has covered the source of each MISFET, and the front face of a drain, as shown in drawing 32 , the silicide layer 43 of low resistance is formed in the front face of the gate electrodes 31a, 31b, and 31c and the source, and a drain (n+ [Mold semiconductor region 41] the mold semiconductor region 39 and p+ the mold semiconductor region 40 and n+). The silicide layer 43 deposits refractory metal films, such as Co (cobalt) film and Ti (cobalt) film, by the sputtering method for example, on the semiconductor substrate 1, and after it subsequently heat-treats the semiconductor substrate 1, makes a refractory metal film, a substrate (Si), and a gate electrode (31a-31c) react and forms Co silicide layer, it forms them by removing an unreacted refractory metal film by wet etching.
[0095] Next, as shown in drawing 33 , after forming contact holes 45, 46, and 47 in the silicon oxide film 44 deposited on the semiconductor substrate 1 by the same method as the gestalt 1 of said operation, the flash memory of the gestalt 2 of this operation carries out abbreviation completion by forming wiring 48-52 in the upper part of the silicon oxide film 44.
[0096] Drawing 34 is the table of the photo mask used by the above-mentioned manufacture method. Among the photo

masks of 13 sheets used at all processes, the photo mask of a proper is two sheets, the object for processing of a silicon nitride film (No.6), and the object for drain formation (No.7), and is dramatically simplified by manufacture of a memory cell.

[0097] Moreover, writing/elimination operating characteristic and the retention property of a flash memory which were manufactured by the above-mentioned method were comparable as the flash memory of the gestalt 1 of said operation.

[0098] (Gestalt 3 of operation) Drawing 35 is the important section cross section of the semiconductor substrate in which the cellular structure of the flash memory of the gestalt of this operation is shown.

[0099] The two-layer film of the silicon oxide film 60 which formed the gate insulator layer by the side of a drain in the silicon oxide film 9 and its lower layer constitutes the memory cell (MISFETQm) of the gestalt 1 of said operation from the gestalt of this operation to constituting the gate insulator layer by the side of a drain from a silicon oxide film 9 of one layer. Moreover, the electric capacity thickness of the gate insulator layer by the side of the drain which consisted of silicon oxide films 9 and 60 two-layer [these] is almost equal to the electric capacity thickness of the gate insulator layer by the side of the source which consisted of silicon oxide films 7 and 9 and a silicon nitride film 8 inserted into them. That is, the gate insulator layer of this memory cell consists of electric capacity thickness (for example, about 17.5nm) with almost equal drain side and source side.

[0100] The configuration and program actuation except the memory cell of the gestalt of this operation having described above are the same as the memory cell of the gestalt 1 of said operation. Moreover, the manufacture method of the memory cell of the gestalt this operation is the same as the manufacture method of the gestalt 1 said operation, except that the process which heat-treats the semiconductor substrate 1 and forms the silicon oxide film 60 increases as 1 **.

[0101] Even when the length which met in the direction of gate length of the gate insulator layer by the side of the source (the silicon oxide film 9, a silicon nitride film 8, silicon oxide film 7) by having made electric capacity thickness of a gate insulator layer almost the same in the whole lower part of gate electrode 10a is changed by dispersion in a manufacture process according to the flash memory of the gestalt of this operation, the actuation capacity of drain current is not changed. Since the drain current at the time of write-in actuation becomes fixed by this, fluctuation of write-in time amount is prevented and it becomes possible to acquire a stable memory cell property.

[0102] (Gestalt 4 of operation) Drawing 36 is the important section cross section of the semiconductor substrate in which the cellular structure of the flash memory of the gestalt of this operation is shown.

[0103] The memory cell of the gestalt 1 of said operation constitutes the whole gate insulator layer of the lower part of gate electrode 10a from a gestalt of this operation to constituting only the gate insulator layer by the side of the source from three layer membranes (the silicon oxide film 9, a silicon nitride film 8, silicon oxide film 7) by the three above-mentioned layer membrane (the silicon oxide film 9, a silicon nitride film 8, silicon oxide film 7). Each thickness of these 3 layer membrane is about 7nm.

[0104] The configuration and program actuation except the memory cell of the gestalt of this operation having described above are the same as the memory cell of the gestalt 1 of said operation. Moreover, the manufacture method of the memory cell of the gestalt this operation is the same as the manufacture method of the gestalt 1 said operation, except that one process of processes which carry out patterning of the silicon oxide film 7 and the silicon nitride film 8, and it leaves only to a source side is skipped. The writing of this memory cell was 1 microsecond.

[0105] (Gestalt 5 of operation) Drawing 37 is the important section cross section of the semiconductor substrate in which the cellular structure of the flash memory of the gestalt of this operation is shown.

[0106] This flash memory constitutes the memory cell from MISFETQc and MISFETQs for selection which are the storage element section. MISFETQc of the storage element section mainly Lower gate oxide 70 of about 8nm of thickness, The gate electrode 73 for writing/elimination which consists of a polycrystalline silicon film formed on the gate insulator layer of the three-tiered structure which consists of a silicon nitride film 71 of about 10nm of thickness, and up gate oxide 72 of about 10nm of thickness (PEG), It consists of the sources and the drains (connection diffusion layer) which were formed in the semiconductor substrate 1 of the both sides of this gate electrode 73.

[0107] The source is n of the low high impurity concentration in which the end section extends to the lower part of the gate electrode 73. - n+ of the mold semiconductor region 74 and the high high impurity concentration formed so that it might offset to the gate electrode 73 It is n+ of the high high impurity concentration in which it consists of mold semiconductor regions 75, and, as for a drain (connection diffusion layer), the end section extends to the lower part of the gate electrode 73. It consists of mold semiconductor regions 76.

[0108] moreover -- selection -- ** -- MISFETQs -- mainly -- thickness -- four -- nm -- about -- gate oxide -- 77 -- the upper part -- forming -- having had -- polycrystalline silicon -- a film -- etc. -- from -- becoming -- selection -- ** -- the gate -- an electrode -- (-- SG --) -- 78 -- this -- the gate -- an electrode -- 78 -- both sides -- a semiconductor -- a substrate -- one -- forming -- having had -- the source (connection diffusion layer) -- a drain -- constituting -- having -- **** . A

drain is n+ of the high high impurity concentration in which the end section extends to the lower part of the gate electrode 78. It consists of mold semiconductor regions 79. The source is n+ of the high high impurity concentration which is the drain of Above MISFETQc. Consisting of mold semiconductor regions 76, the end section has extended to the lower part of the gate electrode 78.

[0109] Program actuation of the above-mentioned flash memory is explained using drawing 38 (operating voltage table of a memory cell). Writing is n of the low high impurity concentration which constitutes some sources by impressing 5V to the drain of MISFETQs for selection, and it impressing 2V to the gate electrode 78, and turning ON (ON) MISFETQs for selection, making the source of MISFETQc of the storage element section into touch-down potential (0V), and impressing 5V to the gate electrode 73. - The peak of field strength is produced near the mold semiconductor region 74. The hot electron generated in this field is injected into the electron trap in a silicon nitride film 71 by this, and writing is performed when the threshold voltage seen from the gate electrode 73 of MISFETQc rises more than 4V. Since this memory cell can control drain current on the voltage impressed to the gate electrode 73, it can control the potential of a substrate and the gate electrode for writing/elimination, and can be written in with lower power consumption compared with the conventional MNOS mold memory cell which pours in an electron completely into a silicon nitride film from a substrate side through a direct tunnel oxide film.

[0110] Elimination actuation impresses 5V to the gate electrode 73 of MISFETQc at -10V, the source, and a well, and is performed by emitting the electron in a silicon nitride film 71. Moreover, read-out actuation impresses 2V to the drain of MISFETQs for selection and the gate electrode 78, and the gate electrode 73 of MISFETQc, and is performed by judging the threshold voltage of MISFETQc.

[0111] (Gestalt 6 of operation) Drawing 39 is the important section cross section of the semiconductor substrate in which the cellular structure of the flash memory of the gestalt of this operation is shown.

[0112] MISFET which constitutes this memory cell consists of a gate electrode 83 which consists of a polycrystalline silicon film formed mainly on the gate insulator layer, and the source and the drain which were formed in the semiconductor substrate 1 of the both sides of this gate electrode 83. The source is n+ of the high high impurity concentration in which the end section extends to the lower part of the gate electrode 83. It is p of the low high impurity concentration (about three 1x1018-1019-/cm) in which it consists of mold semiconductor regions 84, and, as for a drain, the end section extends to the lower part of the gate electrode 83. - n+ of the mold semiconductor region 85 and the high high impurity concentration formed so that it might offset to the gate electrode 83 It consists of mold semiconductor regions 86. Moreover, the gate insulator layer consists of lower gate oxide 80 whose drain side is about 8nm of thickness, a silicon nitride film 81 of about 10nm of thickness, and up gate oxide 82 of about 10nm of thickness to the source side consisting of gate oxide 82 which is about 10nm of thickness. Thus, the memory cell of the gestalt of this operation has the feature in the point of performing hot electron impregnation at the time of writing by the drain side.

[0113] As shown in drawing 40 , read-out and elimination actuation of this flash memory are the same as the memory cell of the gestalt 1 of said operation. On the other hand, writing makes the drain of the selected memory cell touch-down potential (0V), and is performed by impressing the positive voltage of 5V to the gate electrode 83 and the source, respectively.

[0114] Drawing 41 is a graph which shows time amount change of voltage impression for each terminal at the time of write-in actuation. Writing precharges all bit lines to 5V, after charging the common source line of memory block chosen first 5V. Next, after carrying out pressure up only of the selected word line to 5V, only the selected bit line is dropped to 0V. The time amount which dropped these 0V writes in, it is time amount and channel current flows in the direction of a drain from the source of the memory cell chosen into this time amount. As shown in drawing 42 at this time, in order to descend in a low concentration drain (p-mold semiconductor region 85) field, the peak of field strength produces the great portion of potential set as 0V the 5V and drain side the source side at the drain edge. And writing is performed by being accelerated by the lengthwise direction electric field of 5V impressed to the selected word line, and injecting into the electron trap in a silicon nitride film 81 the hot electron generated by this high electric field.

[0115] (Gestalt 7 of operation) Drawing 43 is the important section cross section of the semiconductor substrate in which the cellular structure of the flash memory of the gestalt of this operation is shown.

[0116] This memory cell is n of the low high impurity concentration in which hot electron impregnation at the time of writing is performed by the drain side, and the end section extends to the lower part of the gate electrode 83. - n+ of the mold semiconductor region 87 and the high high impurity concentration formed so that it might offset to the gate electrode 83 Except that the source consists of mold semiconductor regions 84, it has the same cellular structure as the gestalt 6 of said operation.

[0117] Writing is started by precharging all bit lines to 5V, after charging the common source line of selected memory block like the gestalt 6 of said operation 5V. By the way, if the cementation leakage current of the common source line

charged is large since the serviceability of a power supply is restricted when 5V power supply for this writing is an internal electrical power source like the booster circuit formed on the chip, the problem that sufficient voltage cannot be charged will arise. At the gestalt of this operation, it is n of low high impurity concentration to a source side. - Since the electric field of source cementation are eased and leakage current reduction of source cementation and improvement in cementation pressure-proofing are achieved in case the source is charged by having formed the mold semiconductor region 87 at the time of writing, the above problems are avoidable.

[0118] (Gestalt 8 of operation) The important section plan in which drawing 44 shows the cellular structure of the flash memory of the gestalt of this operation, and drawing 45 are A-A' of drawing 44 . It is the important section cross section of the semiconductor substrate which met the line.

[0119] Like the gestalt 1 of said operation, MISFETQm which constitutes the memory cell of the gestalt of this operation constitutes the gate insulator layer by the side of the source from three layer membranes (the silicon oxide film 9, a silicon nitride film 8, silicon oxide film 7), and constitutes the drain side from a silicon oxide film 9 of one layer. On the other hand, bit line DL and a drain (n+ mold semiconductor region 92) are electrically connected through the plug 98 formed in the upper part of a drain. Moreover, the source (n+ mold semiconductor region 92) of two or more memory cells which met in the extension direction of the gate electrode 90 is electrically connected through the source line (SL) constituted by the plug 98 formed in the upper part.

[0120] in order to manufacture the above-mentioned memory cell, it is first shown in drawing 46 -- as -- n mold deep to the semiconductor substrate 1 of p mold by the same method as the gestalt 1 of said operation -- a well 4 and shallow p mold, after forming a well 5 The gate insulator layer from which the source side was constituted from three layer membranes (the silicon oxide film 9, a silicon nitride film 8, silicon oxide film 7) by the front face of a well 5, and the drain side was constituted from a silicon oxide film 9 of one layer p mold is formed.

[0121] The above-mentioned silicon oxide film 7 oxidizes thermally and forms the semiconductor substrate 1 at about 800 degrees C, and the thickness sets it to about 11nm. Moreover, a silicon nitride film 8 is formed with an about 730-degree C heat CVD method, and the thickness sets it to about 10nm. Furthermore, after the silicon oxide film 9 carries out patterning of the above-mentioned silicon nitride film 8 and the silicon oxide film 7 and leaves these films only a source formation field and near the memory cell, it oxidizes thermally and forms the semiconductor substrate 1 at about 800 degrees C, and the thickness sets it to about 15nm.

[0122] Next, as shown in drawing 47 , after depositing about 100nm of thickness, and the polycrystalline silicon film of 2x1020/of about three Lynn concentration cm on the upper part of the silicon oxide film 9 with a CVD method and, depositing the silicon nitride film 93 of about 200nm of thickness with a CVD method subsequently to the upper part, the gate electrode 90 which consisted of above-mentioned polycrystalline silicon films is formed by carrying out patterning of these films by the dry etching which used the photoresist film as the mask.

[0123] Next, it is p by using as a mask the photoresist film which prepared the aperture in the source formation field, and carrying out the ion implantation of the p mold impurity (boron) to a well 5 p mold from the direction of 30 slant on condition that acceleration energy 20keV and 1x1013/cm2 of doses, as shown in drawing 48 . - The mold semiconductor region 91 is formed. then, the thing done for the ion implantation of the n mold impurity (arsenic) all over a memory cell array field on condition that acceleration energy 50keV and 2x1015/cm2 of doses -- p mold of the both sides of the gate electrode 90 -- n+ which constitutes the source and a drain in a well 5 The mold semiconductor region 92 is formed.

[0124] Next, as shown in drawing 49 , it is a silicon nitride film (after depositing, the sidewall spacer 94 is formed in the side attachment wall of the gate electrode 90 by carrying out anisotropic etching of this silicon nitride film.) with a CVD method on the semiconductor substrate 1. At this time, the source and the gate insulator layer which has covered the front face of a drain are also etched simultaneously.

[0125] Next, as shown in drawing 50 , after depositing the silicon oxide film 95 with a CVD method on the semiconductor substrate 1, by using as a mask the source and the photoresist film which prepared the aperture in the upper part of a drain, and etching this silicon oxide film 95, a contact hole 96 is formed in a source line formation field including the upper part of the source, and a contact hole 97 is formed in the upper part of a drain.

[0126] At the process which etches the above-mentioned silicon oxide film 95, since the sidewall spacer 94 of the silicon nitride formed in the side attachment wall of the gate electrode 90 functions as an etching stopper, the above-mentioned contact holes 96 and 97 are formed by self align (self aryne) to the space of the gate electrode 90. Since the doubling additional coverage of contact holes 96 and 97 and the gate electrode 90 becomes unnecessary by this, the space of the gate electrode 90 can be designed with the minimum processing size.

[0127] Next, as shown in drawing 51 , a source line (SL) is formed in the interior of a contact hole 96, and a plug 98 is formed in the interior of a contact hole 97. the front face of this polycrystalline silicon film after a source line (SL) and a

plug 98 deposit on the upper part of the silicon oxide film 95 the polycrystalline silicon film which doped n mold impurity with a CVD method -- chemical mechanical polishing (CMP) -- it forms by carrying out flattening by law.
[0128] Then, after depositing the silicon oxide film 99 on the upper part of the silicon oxide film 95 with a CVD method, aluminum alloy film is deposited on the upper part of the silicon oxide film 99 by the sputtering method, and the flash memory of the gestalt of this operation shown in said drawing 44 and drawing 45 carries out abbreviation completion by carrying out patterning of this aluminum alloy film by the dry etching which used the photoresist film as the mask, and forming bit line DL.
[0129] since the space of the gate electrode 90 can be designed with the minimum processing size according to the gestalt of this operation -- 0.3 micrometer gate length -- cel area -- 0.5micrometerx0.4micrometer=0.2micrometer2 up to -- it was reducible. Moreover, the write-in time amount of a memory cell is 5 microseconds, blanking time is 10 mses, and the fully stabilized same retention property as the gestalt 1 of said operation was able to be checked.
[0130] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of said operation, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of said operation, and does not deviate from the summary.
[0131] The nonvolatile memory of this invention has the simple cellular structure, and a manufacture process and application to LSI which loads together nonvolatile memory and Logic LSI on the same semiconductor substrate since it is simple are easy for it.
[0132]
[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated by this application is explained briefly.
[0133] Since the nonvolatile memory of this invention consists of MISFET(s) with a single memory cell, it does not make the area of the circumference circuit which can perform writing/elimination actuation comparatively simple, and needs it increase. Moreover, a manufacturing process is also simple.
[0134] The nonvolatile memory of this invention impresses positive voltage to a gate electrode and a drain in the case of write-in actuation, since the method which injects into the electron trap in a silicon nitride film the hot electron generated near the source is used for it, when the source of touch-down potential and the gate inter-electrode potential difference become large, its injection efficiency improves and the actuation of it by the low battery is attained more compared with the conventional cellular structure.
[0135] Since the manufacture method of the nonvolatile memory of this invention forms the gate insulator layer by the side of the source of a memory cell (insulator layer of three layers which consists of a silicon oxide film, a silicon nitride film, and a silicon oxide film) by self align (self aryne) to a gate electrode, it can design in a cel area equivalent to the conventional floating-gate mold memory cell, and nonvolatile memory excellent in scalability can be realized.

[Translation done.]

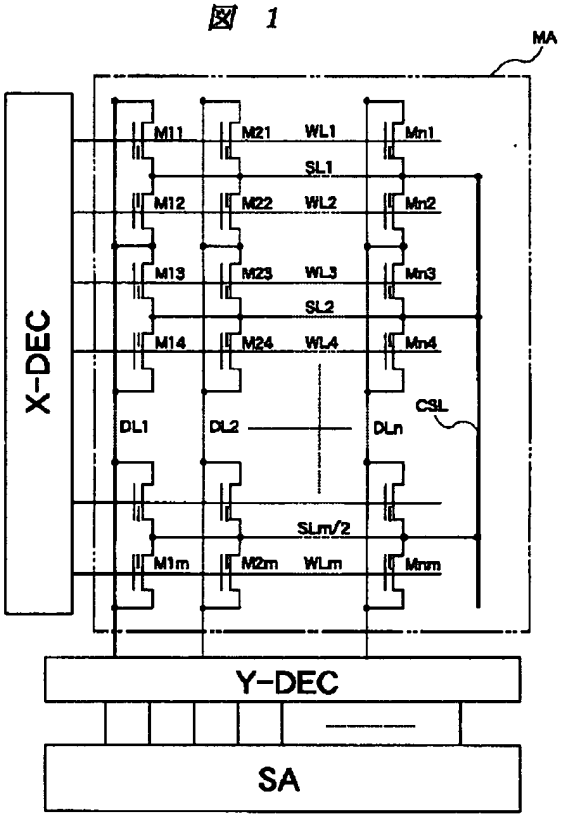
* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

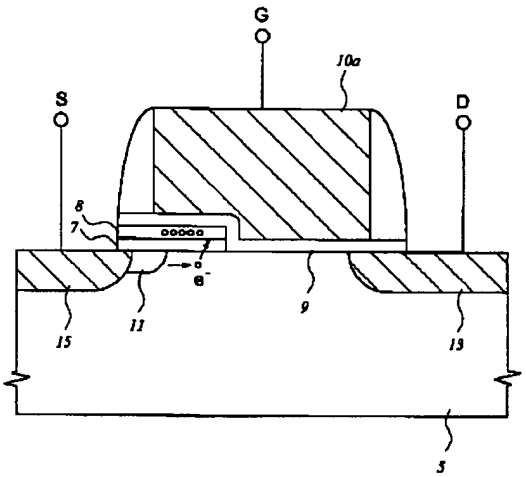
[Drawing 1]

図 1



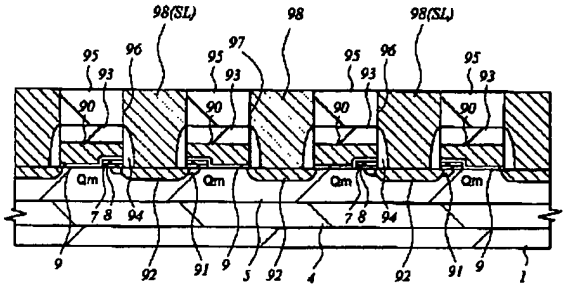
[Drawing 4]

図 4



[Drawing 51]

図 51



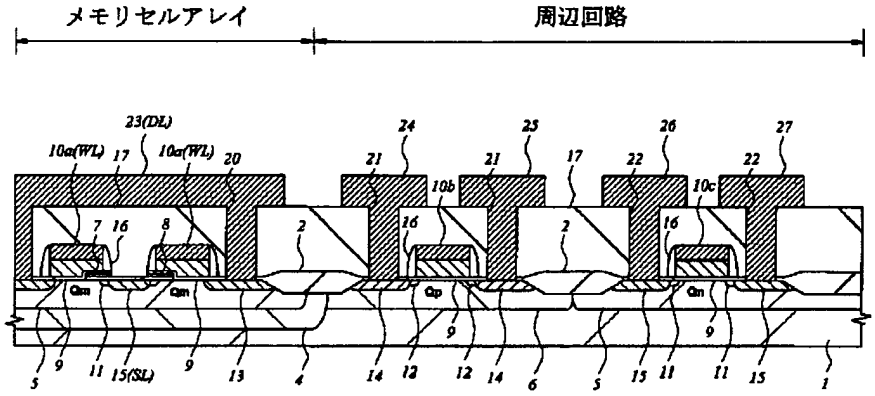
[Drawing 5]

図 5

端子	ビット線（ドレイン電圧）		ワード線（ゲート電圧）		ソース線	ウエル
	選択	非選択	選択	非選択		
書込み	5V	0V	5V	0V	0V	0V
消去	0V	0V	-10V	0V	5V	5V
読み出し	2V	0V	2V	0V	0V	0V

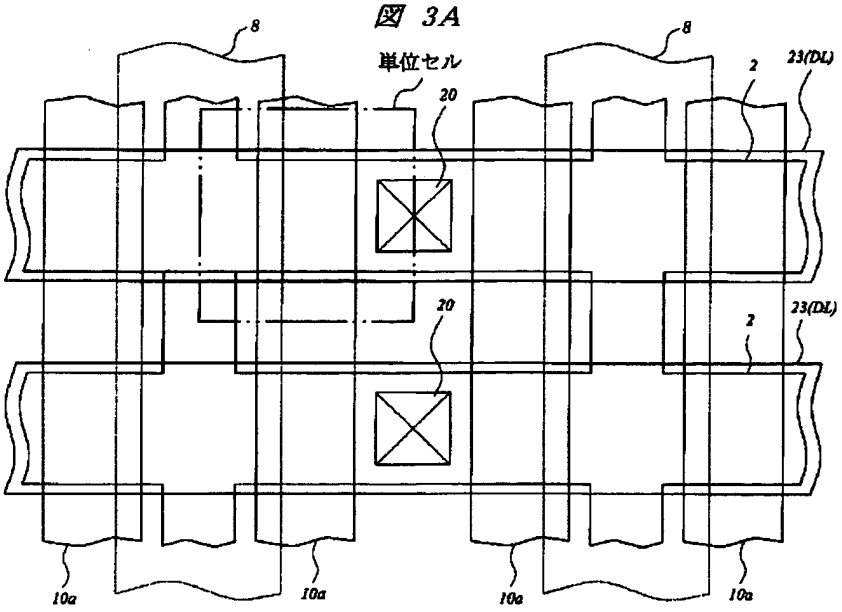
[Drawing 2]

図 2



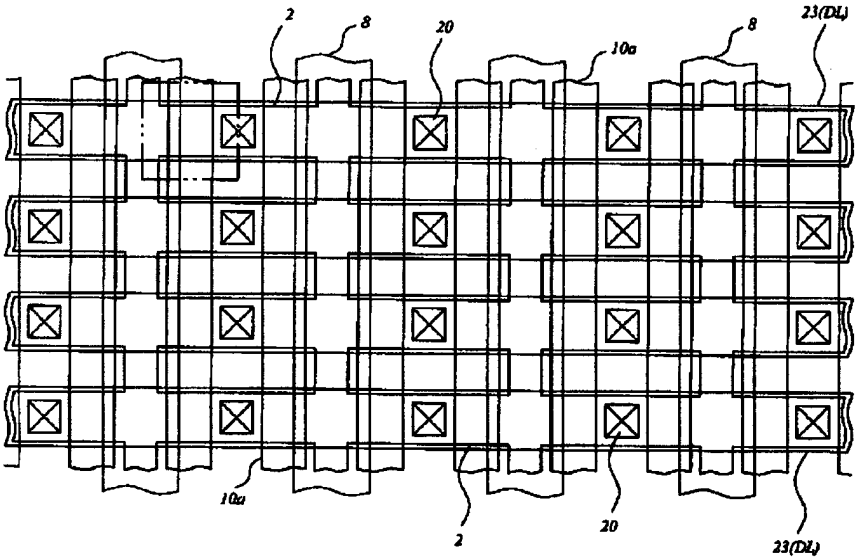
[Drawing 3 A]

図 3A



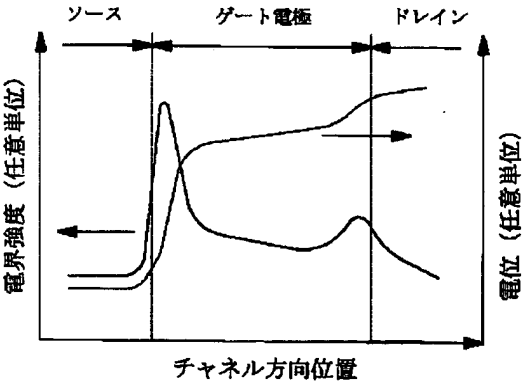
[Drawing 3 B]

図 3B



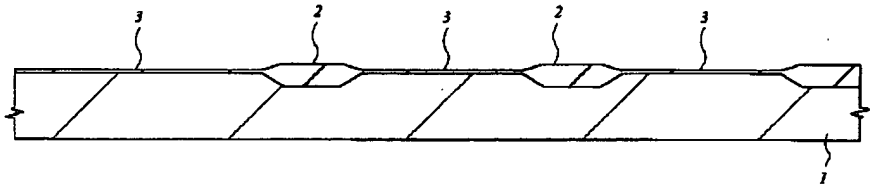
[Drawing 6]

図 6



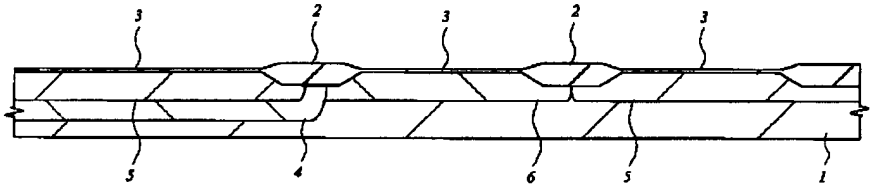
[Drawing 7]

図 7



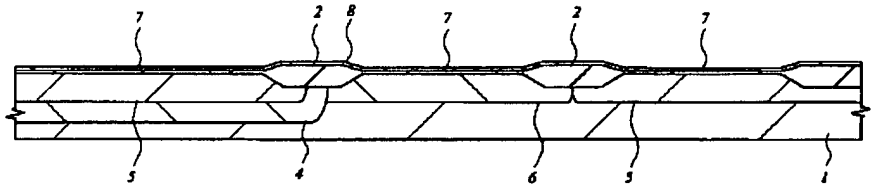
[Drawing 8]

図 8



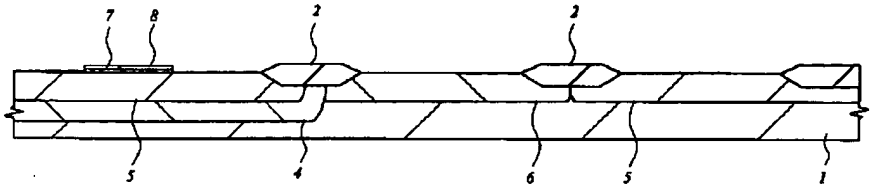
[Drawing 9]

図 9



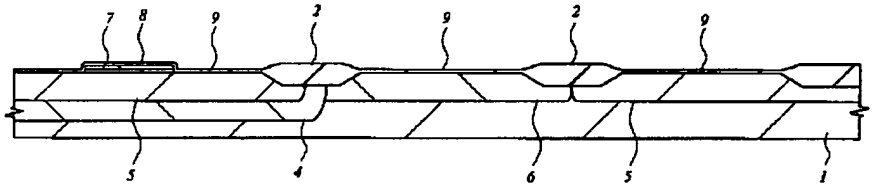
[Drawing 10]

図 10



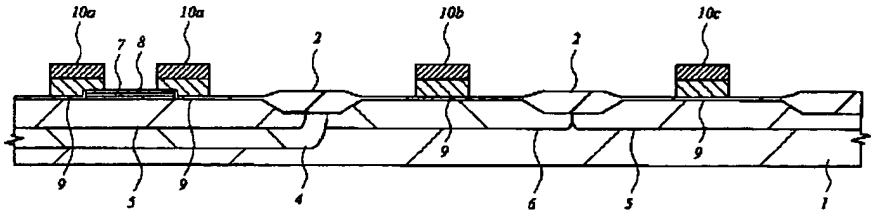
[Drawing 11]

図 11



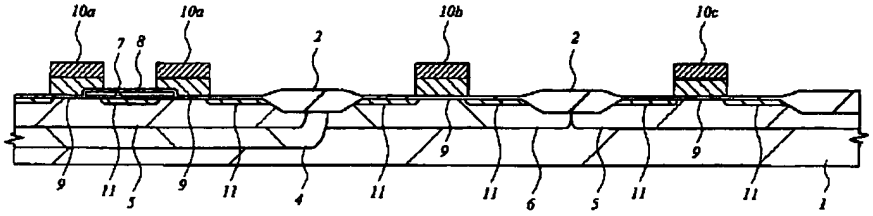
[Drawing 12]

図 12



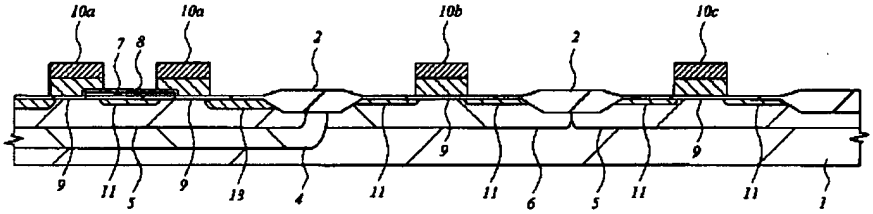
[Drawing 13]

図 13



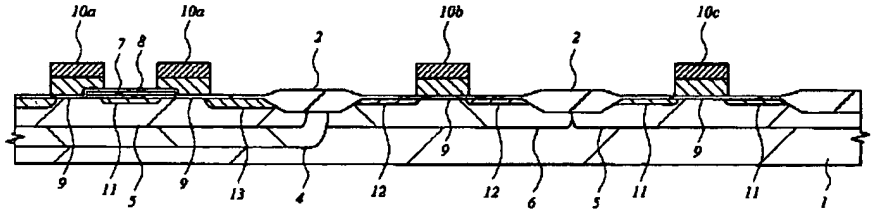
[Drawing 14]

図 14



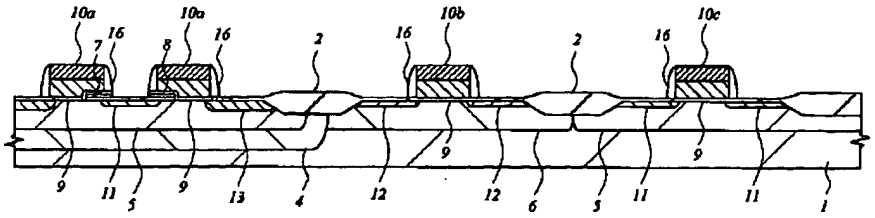
[Drawing 15]

図 15



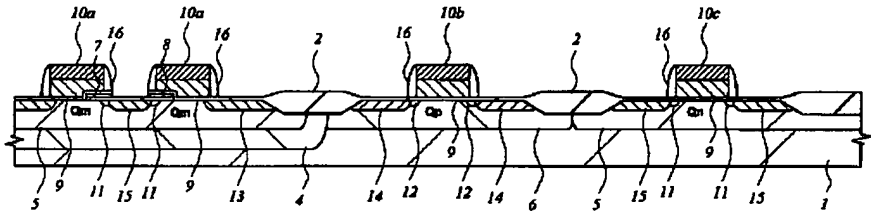
[Drawing 16]

図 16



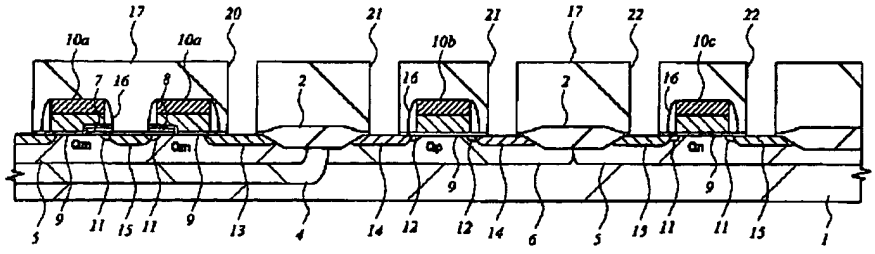
[Drawing 17]

図 17



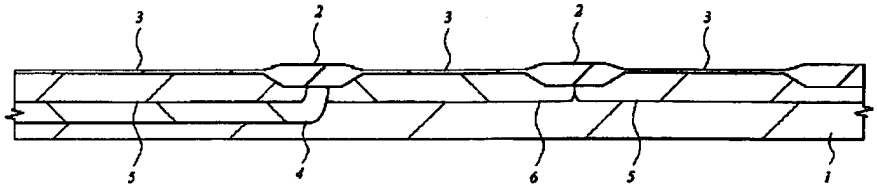
[Drawing 18]

図 18



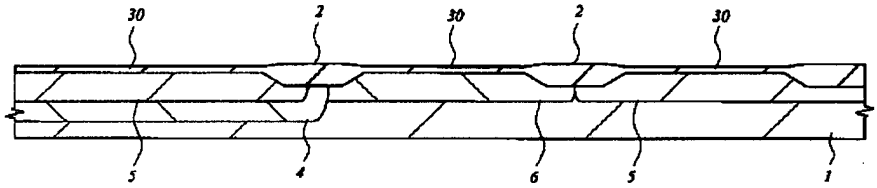
[Drawing 19]

図 19



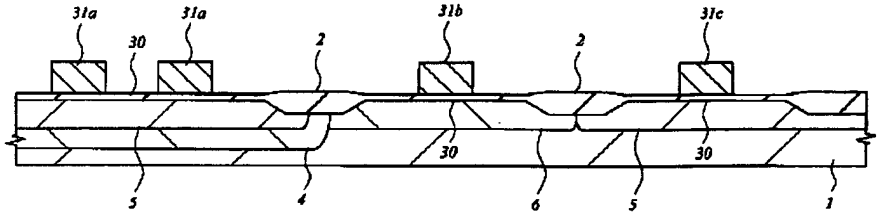
[Drawing 20]

図 20



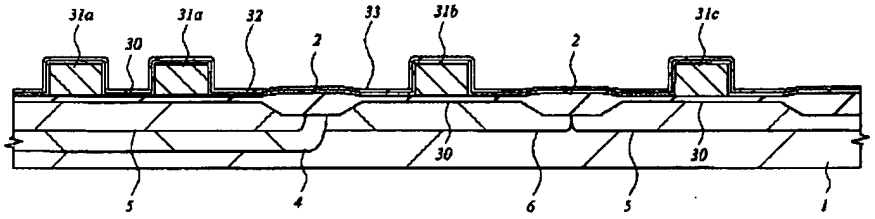
[Drawing 21]

図 21



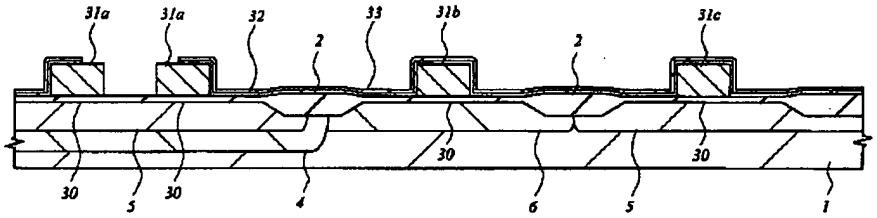
[Drawing 22]

図 22



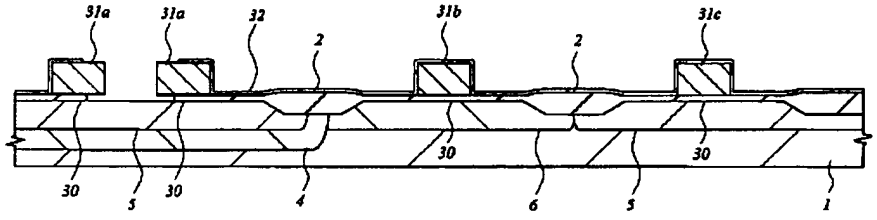
[Drawing 23]

図 23



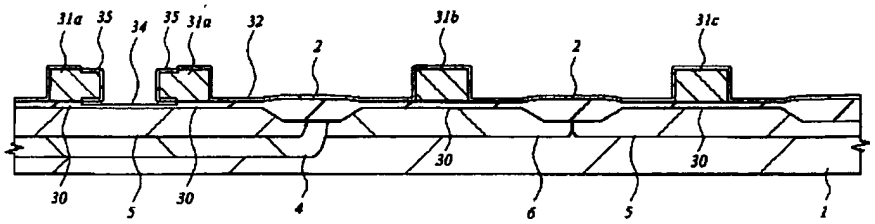
[Drawing 24]

図 24



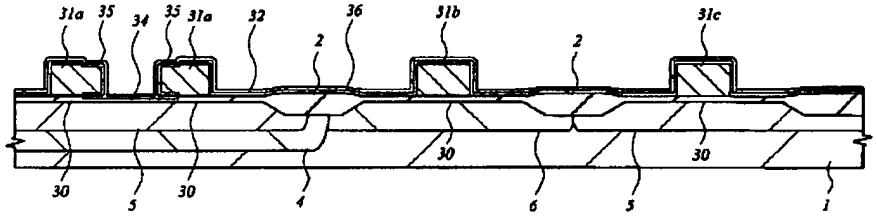
[Drawing 25]

図 25



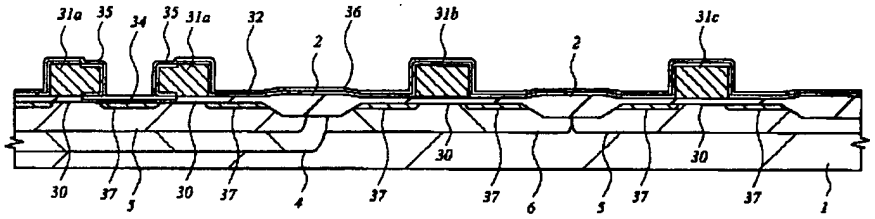
[Drawing 26]

図 26



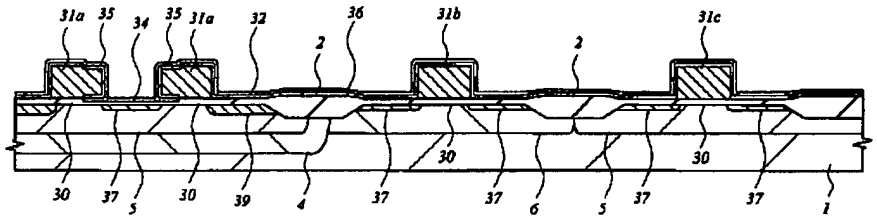
[Drawing 27]

図 27



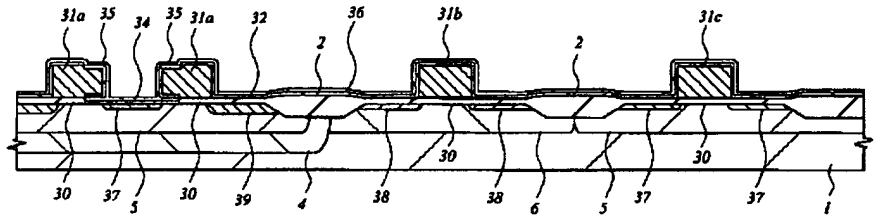
[Drawing 28]

図 28



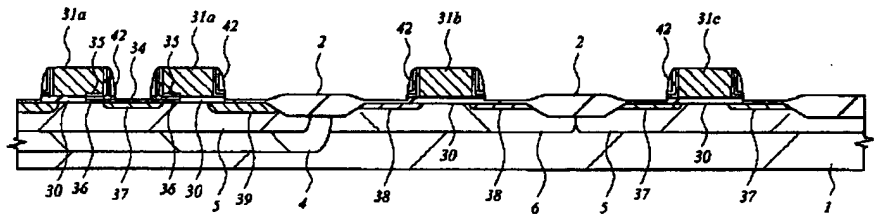
[Drawing 29]

図 29



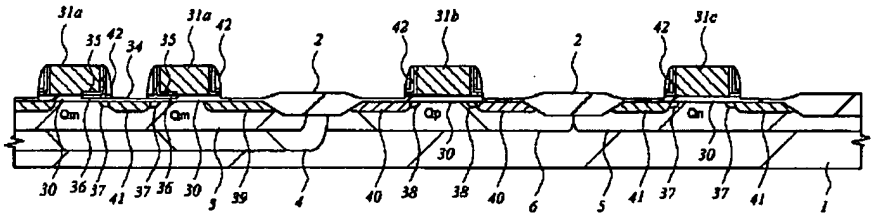
[Drawing 30]

図 30



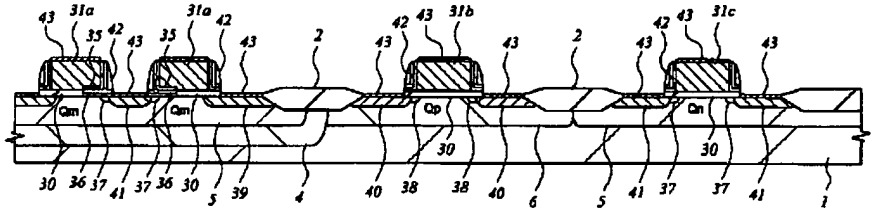
[Drawing 31]

図 31



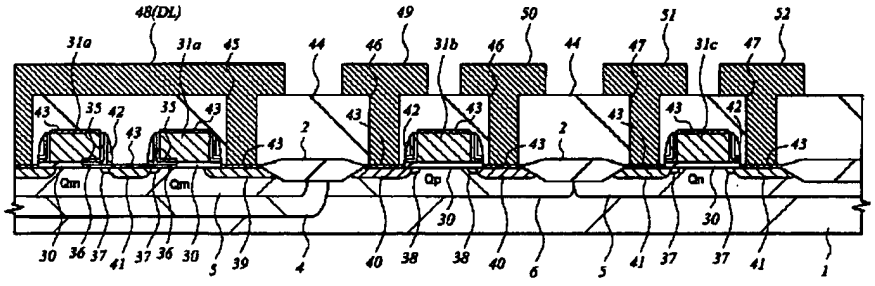
[Drawing 32]

図 32



[Drawing 33]

図 33



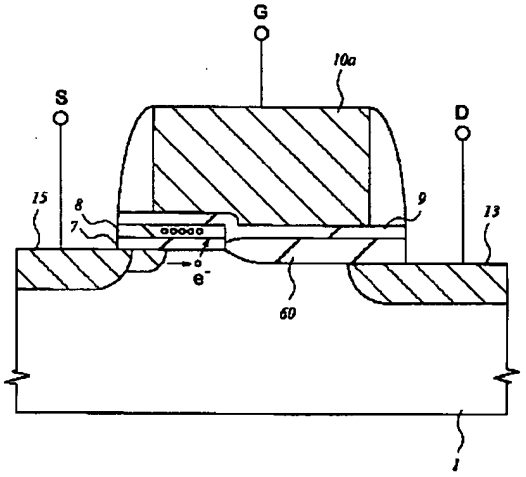
[Drawing 34]

図 34

1. アイソレーション形成
2. 深いｎ型ウエルインプラ
3. 浅いｎ型ウエルインプラ
4. ｐ型ウエルインプラ
5. ゲート電極加工
6. メモリセル部分開口
7. メモリセル部ドレインインプラ
8. 周辺ｐＭＯＳ低濃度ソース、ドレインインプラ
9. ｎ+型半導体領域インプラ
10. ｐ+型半導体領域インプラ
11. コンタクトホール開孔
12. 第１メタル配線加工

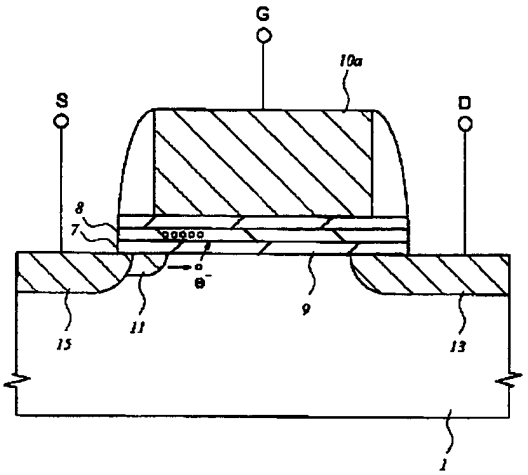
[Drawing 35]

図 35



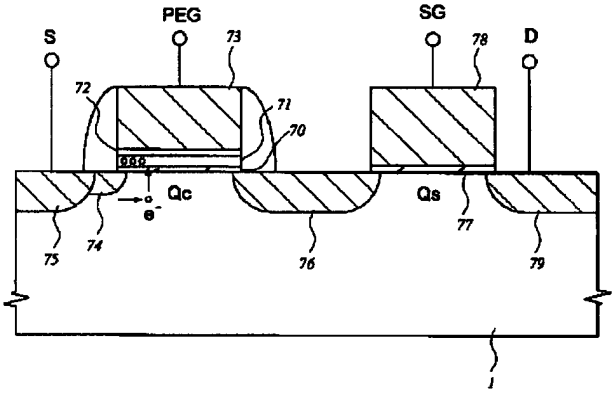
[Drawing 36]

図 36



[Drawing 37]

図 37



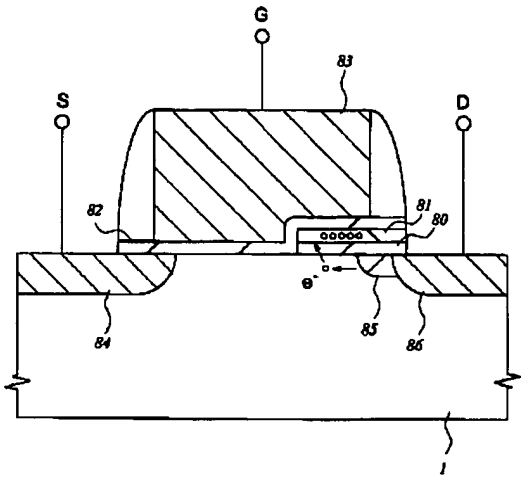
[Drawing 38]

図 38

端子	ビット線 (D)		ワード線 (SG)		書込消去線 (PEG)		ソース線 (S)	ウエル
	選択	非選択	選択	非選択	選択	非選択		
書込み	5V	0V	2V	0V	5V	0V	0V	0V
消去	0V	0V	0V	0V	-10V	0V	5V	5V
読み出し	2V	0V	2V	0V	2V	0V	0V	0V

[Drawing 39]

図 39



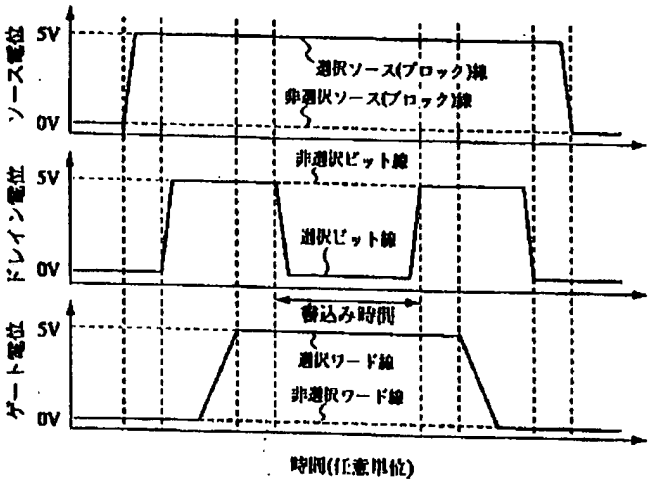
[Drawing 40]

図 40

端子	ビット線（ドレイン電圧）		ワード線（ゲート電圧）		ソース線	ウエル
	選択	非選択	選択	非選択		
書込み	0V	5V	5V	0V	5V	0V
消去	0V	0V	-10V	0V	5V	5V
読み出し	2V	0V	2V	0V	0V	0V

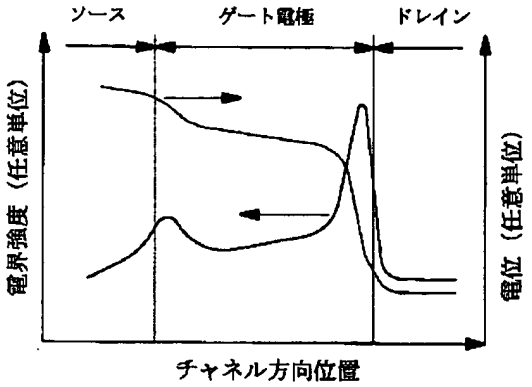
[Drawing 41]

図 41



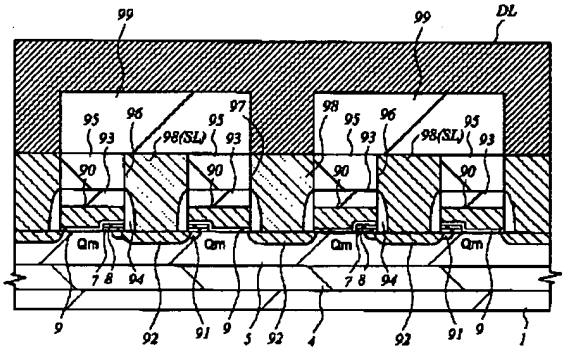
[Drawing 42]

図 42



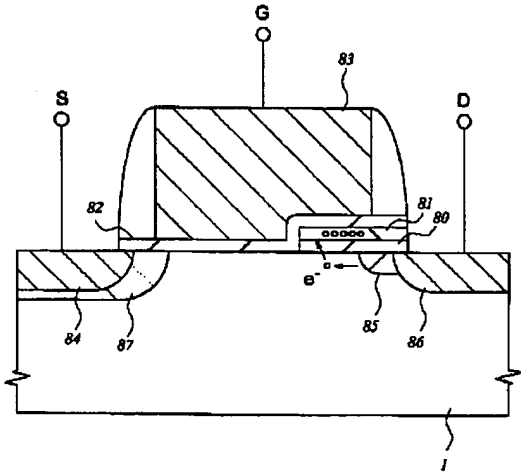
[Drawing 45]

図 45



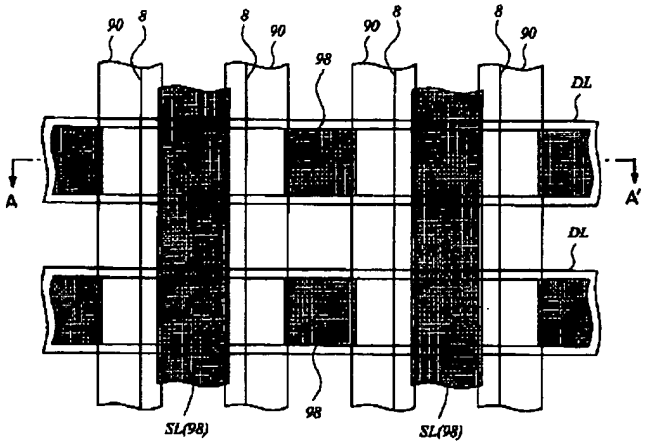
[Drawing 43]

図 43



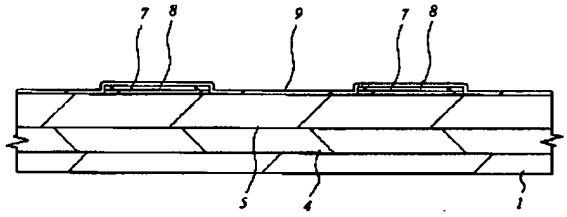
[Drawing 44]

図 44



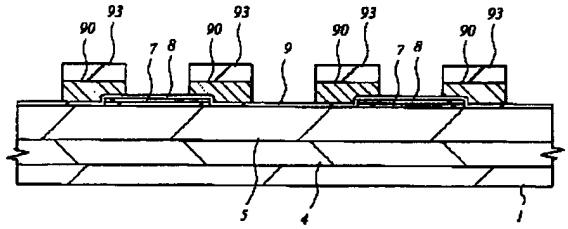
[Drawing 46]

図 46



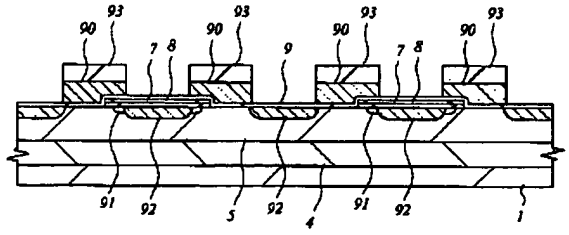
[Drawing 47]

図 47



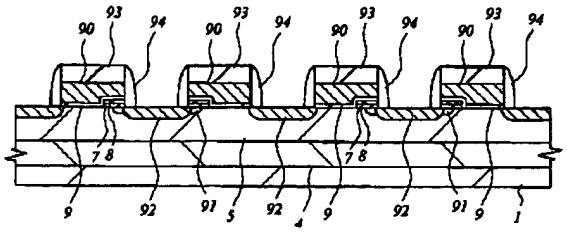
[Drawing 48]

図 48



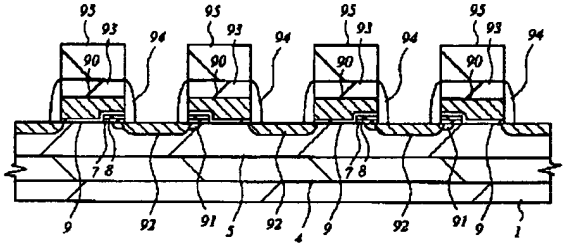
[Drawing 49]

図 49



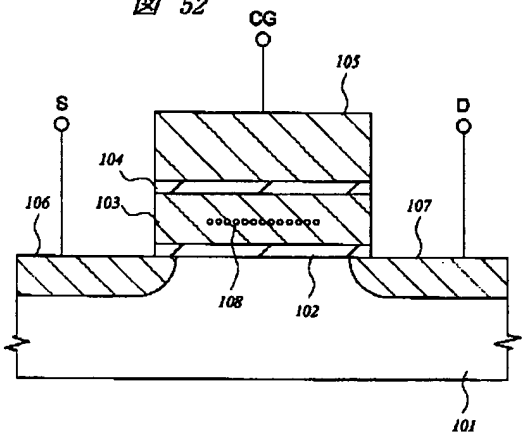
[Drawing 50]

図 50



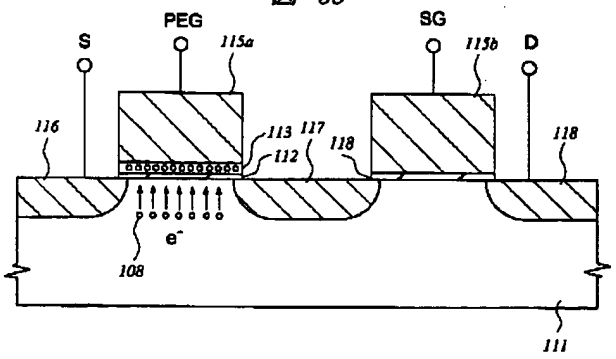
[Drawing 52]

図 52



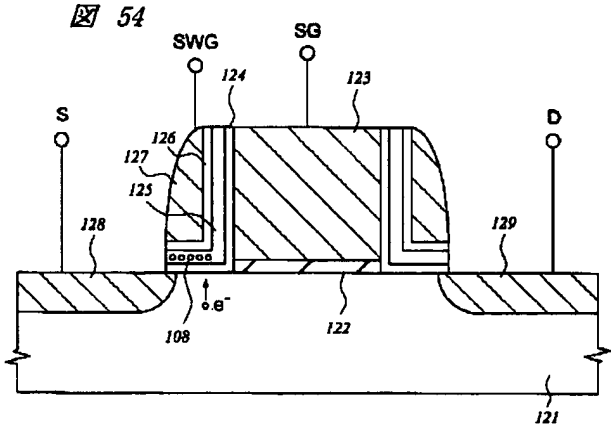
[Drawing 53]

図 53



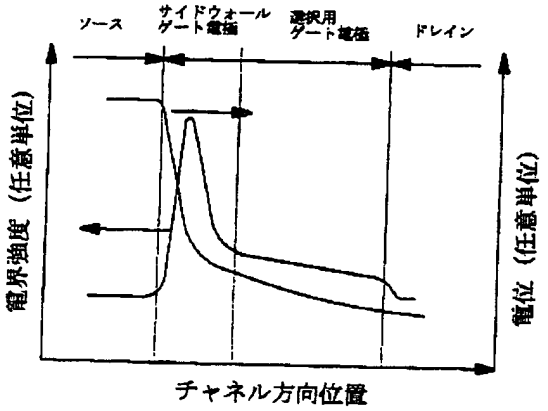
[Drawing 54]

図 54



[Drawing 55]

図 55



[Translation done.]